Original Research Article

Characterisation of Defects Induced by Ion-implantation Processing of P^+N Shallow Junction Devices.

Abstract.

The DLTS technique was used to characterise defects induced by ion-implantation processing in P^+N shallow junction devices. BF_2 implantation was carried out on silicon diodes pre-armophized by Ge at different energies. The variation of implantation energy and its effects on the type of defects generated and concentration of those defects across the device were of were evaluated. From an electronic point of view, defects were categorised into two groups – that is shallow level and deep level defects. The results revealed that the higher the implant energy the more defects, of all of both types, generated in the device. Effectively, concentrations of both shallow and deep level defects in the devices increased as implant energy increased from 30 to 150 keV. The results also reveal that for low implant energy (30 keV) the defects are mainly the shallow level type and defect concentration decreases with depth below junction. High energies (60 and 150 keV) show more or less constant defect concentration across the sample thickness or depth.

Keywords: Transient Spectroscopy, Ion-implantation, Deep level defects, Shallow level defects.

1.1 . INTRODUCTION

The emerging “miniaturized” technology in the electronic industry is manufacturing miniaturized semiconductor devices to improve speed, reduce power consumption and allow for more dense packing of transistors on chips. A semiconductor device is a system composed of manifold materials and whose functionality depends on the contacts between these materials [1]. Virtually for all semiconducting devices the source material has to undergo numerous fabrication processes to achieve desired electrical, optical, and other functional properties. Concomitantly, those fabrication steps introduce defects in the semiconductor lattice. Even modern processing techniques, such as semiconductor growth, plasma etching, annealing, metallization, particle irradiation and doping (through ion implantation and thermal diffusion) are known to introduce imperfections into the crystalline structure of the semiconductor [2,3]. Hence, semiconductor materials, like all other materials, exhibit different types of defects traceable to the fabrication processes they would have gone through [4]. Generally, the electronic industry is particularly concerned with two types of electronically active defects found in semiconductors – namely, shallow level defects and deep level defects (i.e. shallow levels and deep levels). Deep levels have highly localized wave functions, are found deeper in the bandgap than dopant levels, have higher ionization energies resulting in reduced contribution to free charge carriers, and can act as traps or recombination centres in semiconducting materials depending on the capture cross-section of the electrons and holes. The traps reduce free carriers in semiconductors while recombination centres introduce generation-recombination currents in rectifying devices. The trap-induced carrier reduction can be positively utilised to form areas of high resistivity for device isolation [5]. On the other hand, the shallow levels are sited near the valence-band for acceptors and near the conduction-band for donors and are ionized at room temperature (i.e. have low ionization energies). They are normally induced by presence of impurity elements used as dopants in semiconductor and provide free carriers to form n-type or p-type semiconductor [5]. All types of defects can have positive or negative effects on the performance of the materials or devices and more often a combination of both effects. Hence, it is not uncommon for some controlled amounts and types of defects to be deliberately introduced into material crystalline structures to enhance or induced some desirable attributes. However, as already highlighted, in most cases defects are arise inadvertently manufacturing processing. In the electronic industry, some common negative impacts of defects include, the action of deep levels as recombination centres shortening non-radiative lifetime of charge-carriers in solar cells [5]; reduction of light emission efficiency, decreasing diffusion length and reduction of breakdown voltage in diodes; and early failures and redundant leakage current in p-n junction devices [6, 7]. The positive scenarios include absorption of low energy photons in the semiconductor band-gap (that is, enhancement or creation of impurity photovoltaic effect), especially by controlled induced of defects; and acting as efficient recombination centre in fast switching silicon power devices [8].

Suffice to say, defect-free semiconductors are hardly ever exploited in the electronic industry In practice, pure semiconductor crystals do not exist and real crystals always deviate from their presumed perfect structures and/or behaviours due to presence of defects. Generally, in semiconductors, defects give rise to an energy band in the band-gap, but the predominant impacts of any defect depends on the material, the nature of defect and the material property under consideration. Therefore, knowledge of characteristics of defects to achieve the desired property of any semiconductor device is essential in design and fabrication of the device [9]. Actually, the miniaturisation of semiconductor devices, has even made the devices more sensitive to presence of defects in very minute concentrations. Therefore, it has also become even more imperative to identify and control the defects in semiconductor substrates, so as to reduce or eliminate those that are detrimental while retaining or enhancing those that are beneficial [3]. The use of traditional optical techniques in studying semiconductors defects, especially deep level defects, is now known to have serious limitations. The more modern techniques, such as the Deep Level Transient Spectroscopy (DLTS) technique have become the methods of choice for studying and characterising defects in semiconductors.. The DLTS technique, first described by Lang, is a powerful, sensitive, and non-destructive spectroscopic junction capacitance method [2,10]. The technique can measure defect concentrations down to as low as 1 defect per 10^{10} silicon atoms, while in good samples it can also detect traps down to 10^{8} mc^{-3} [11]. Furthermore, DLTS analyses can reveal crucial information about the nature (e.g. energy position in band-gap) as well as the effects of the defects [12]. As such, DLTS is one of the few techniques currently capable of probing the traps in the band-gap introduced by ion implantation of dopants. The other major advantage of the technique is its compatibility to various kinds of space-charge-based devices across a wide spectrum, from simple Schottky barrier diodes (SBD) and p-n junctions and metal-oxide-semiconductor (MOS) structures to more complex device structures [13]. It is worth emphasizing that the DLTS technique operates on the principle of energy levels of the deep level traps being affected by the bending of the energy bands at the interface between the two materials for instance semiconductor or sample and metal contact. The metal-semiconductor interface forms a Schottky barrier diode, and the traps are filled or emptied by varying the extent of the band bending applied biases. That variation has an effect on the capacitance of the diode which can be measured together with the analysed signal to evaluate the concentrations and characteristic of defects present in a material [12]. The main objective of this research was to identify and characterise defects introduced by ion-implantation fabrication of $P^{+}N$ shallow junction devices using the DLTS technique.

2. METHODOLOGY

2.1. Sample Source and Specifications.

Fabrication and measurements for the diodes were done at the Laboratoire d’Analyse et d’Architecture de Systems (LAAS-LNRS) in France; and the diodes were fabricated as outlined by R. Duffy *et al* [14]. Four types of Cz silicon (100) rectangular diodes, labelled P21, P16, P10, and P06, whose structures shown in Fig. 1 below, were used in this investigation. The pn-junction devices were formed by implanting 15keV BF_2 in the n-type Si substrate. The reference sample P21, had a P^+ region formed by BF_2 implantation followed by annealing at 950℃ for 15 seconds. The other three sample diodes, P06, P10 and P16, were initially subjected to implantation with pre-amorphized Germanium (Ge) at different depths and then followed same treatment as P21, forming P^+N junctions. Post-implantation annealing was done for dopant activation. Table.1 gives a detailed summary of these samples' implantation conditions, junction depths and amorphous/crystalline (a/c) depths. The substrate (n-region), $N_d = 2\times 10^{15}\ cm^{-3}$. Different sizes were used for each sample PL1, PL2, PL3, PL4 and PL5 as tabulated in Table.2

Table.1: Sample details for P^+N junction diodes

Sample ID	**Implantation Conditions**	**Junction Depth(nm)**	**a/c depth (nm)**
	All annealed at 950℃ / 15s after implantation		
P21	BF_2 15 keV 10^{15} cm^{-2} (only)	80	0
P16	Ge 30 keV 10^{15} at. cm^{-2} + BF_2 15 keV 10^{15} at. cm^{-2}	70	50
P10	Ge 60 keV 10^{15} at. cm^{-2} + BF_2 15 keV 10^{15} at. cm^{-2}	65	80
P06	Ge 150 keV 10^{15} at. cm^{-2} + BF_2 15 keV 10^{15} at. cm^{-2}	50	180

Table.2: Diode identity (ID) and the corresponding area and perimeter.

Diode Size ID	**Area (μm^2)**	**Perimeter (mm)**
PL1	39900	1.030

PL2	108150	1.355
PL3	327850	2.450
PL4	1013100	4.528
PL5	3136900	7.480

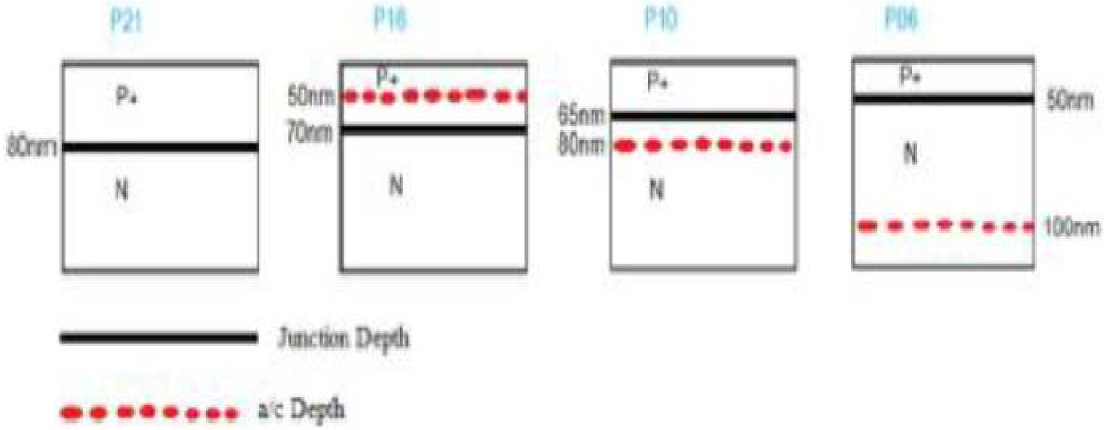

Fig. 1: Schematic diagrams of diode structure showing the position of the EOR defects with respect to junction depth.

Prior to deposition of Schottky contacts, the samples were degreased in boiling trichloroethylene and rinsing was done using boiling isopropanol and de-ionised water. Titanium (Ti) was used as the metal contact. Standard lithography and etching was then applied.

2.2. Experimental Work

The DLTS system was automated using LABVIEW and operated in I-V and C-V measurements. Measurements were carried out under the following conditions: forward-bias voltage was varied from 0V to 1V, reverse-bias voltage was from 0V to -10V, time window was set at 12.5 ms and rate window of 12.5 s^{-1} was applied. The DLTS system consisted of the following key components: a cryostat in which the sample is attached, with temperature controlled by a Lake Shore 340 temperature controller; a fast 1MHz range Boonton 7200 capacitance meter with 100mV, 1Mhz alternating current voltage to monitor thermal emission after excitation by a pulse generator - he Boonton 7200 has a quick response and a recovery time of less than 50µs after overload condition [15]; and a pulse generator to supply a filling pulse to the sample which is followed by a constant quiescent reverse bias during which the capacitance of the sample is observed. In addition, an Agilent 33120A pulse generator supplied the main timing signal and drove fast pulse switches and lasers.

Apart from the above ready-made instruments, reed relays with short switching times (<0.1ms) and minimal contact bounce were applied to connect the pulse generator directly to the sample while disconnecting the meter simultaneously. The settings were such that a sample was kept connected by setting the timing of the reed relays such that the capacitance meter was only disconnected once the pulse generator was connected and there was no contact bounce from the relay. In a like manner after pulse application, the pulse generator was disconnected after the capacitance meter reconnection. The circuit accommodated pulses as short as 50 ns to pass without considerable alteration. An accurate trigger was required for the multimeter to start measuring and ensuring that the same reference point is used for all measurements. Additionally, when filling pulses of different lengths are applied, the multimeter should always be triggered at an instant relative to the trailing edge of the filling pulse. The derivative of the filling pulse was triggered using voltage follower as a buffer connected to a differentiator. The output of the differentiator was fed into a voltage comparator followed by a monostable timer to eliminate false triggering due to oscillations after the initial trigger pulse. The multimeter and an oscilloscope (set up trouble-shooter) were triggered by the output of this circuit. Data was transferred during measurements from the multimeter top the computer in real time by (General Purpose Interface Bus) GPIB interface. The maximum transfer rate required for measurements was 200kB/s. The high transfer rate was achieved by using Windows and Lab View to control and programme all measuring instruments. The required DLTS pulse to the arbitrary waveform generator was downloaded by the software. Sampling rate, resolution and aperture time settings were set on the multimeter and the averaged acquired signal was saved to disk. The smoothed capacitance data gave DLTS spectra by simulating the action of a lock-in amplifier being swept over a frequency range. The DLTS signal was obtained using

$$S(\tau) = \frac{1}{\tau}\int_0^\tau C(t)sin\left(\frac{2\pi t}{\tau}\right)dt$$

Sigma Plot was used for further manipulation of the signal such as subtraction and peak detection. Fig 2, below is an over simplified block diagram of the above describe DTLS system setup.

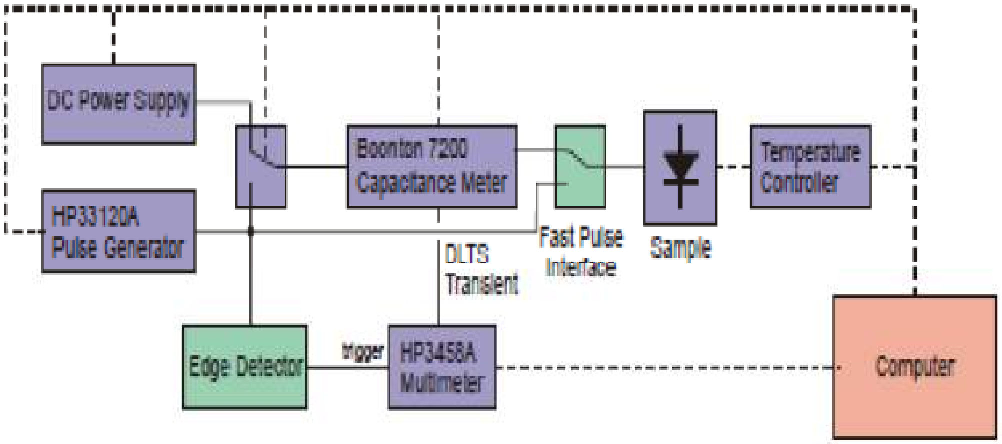

Fig. 2: A block diagram of the DLTS system showing the main components [15]

3. RESULTS AND DISCUSSION

3.1. Defects characterisation

Fig 3 below, are the DLTS spectra for reference sample (P21) and the three experimental samples - P06, P10 and P16. The DLTS spectrum gives positive and negative peaks for electron trap (defect) and hole trap (defect), respectively. The positive DLTS signals (Fig 3) indicate deep levels which are majority carrier (electron) traps in the n-region. The reference sample shows only one defect level E (0.24), which is an electron trap located 0.24 eV below the conduction band. The defect level E (0.24) appears as a shoulder in the experimental samples, especially in samples P06 and P10.

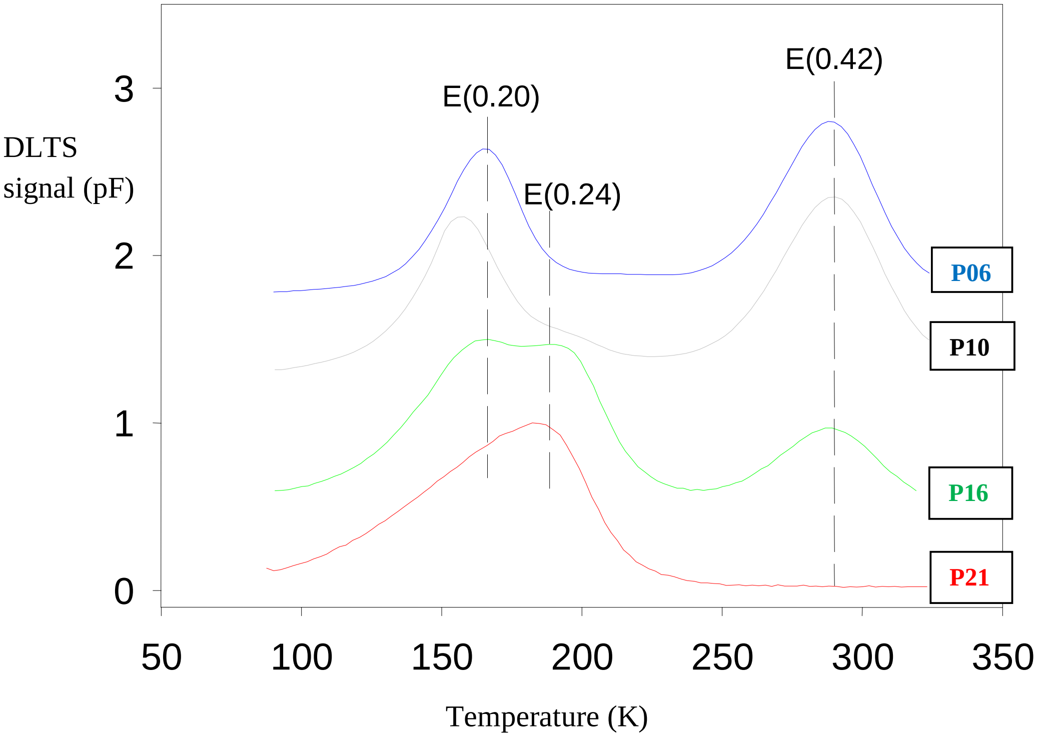

Fig 3: DLTS spectra for P21, (P06), (P10) and (P16)

Two new electron traps - E (0.20) and E (0.42) - absent in the reference sample, are observed in in all the three experimental samples. These electron traps E(0.20), E(0.24) and E(0.42) are electrically active defects present, and have the potential to affect the parameters of the substrate/ semiconductor and affect the fabricated electronic device. This is of interest because the reference (un-implanted) sample has a junction depth zero-no amorphous/ crystalline was formed but the other 3 samples irradiated with Ge had amorphous/ crystalline region at different depths depending on implantation energy. Notably, the signal height (for individual plots, relative to their respective background base-line) does not change with the implantation energy. The signal height has the same order of magnitude for all the samples although they were subjected to different Ge implantation energies.

Of key significance is the defect level E (0.42), particularly for two following reasons. Firstly, it is of it is close to the Si mid-bandgap (0.6 eV), which increases probability of it being electron-hole recombination centre. Secondly, it was not present in the reference sample, but only in all the other samples, hence, it is clearly as result of Ge ion implantation. The increasing height which is proportional to defect concentration, therefore Ge implants energy shows some direct correlation with defects concentration. The defect level E (0.42) is can only be associated with Ge implantation since it is not observed in P21. The defect intensity as denoted by peaks (Fig. 3) and defect concentration (Table 2) increases with increasing implantation energy. Also, the increase in concentration with accelerating voltage of implantation indicates that, the defects are end of range dislocation loops. The nature of the defects could be viewed as a result of the amorphising implants creating a large number of Si interstitials beyond the amorphous/crystalline interface which upon annealing precipitates into extended defects-loops. The fact that the defect concentration increases with implantation energy is also a reflection of a concomitant increase in the number of interstitial Si involved in the end of range defects as the implant energy increases. The high concentration of excess self-interstitial Si introduced by implant energies is responsible for the displacement of a/c interface. Furthermore, the end of range defects location depth also increases with increase in implant energy indicating that the damage caused by higher energy implants extends more deeply with an effect of pushing down the a/c interface.

A plot of defect concentration against depth below the junction for dominant level E(0.42) is presented in Fig 4. The plot reveals that the concentration of the defects varies marginally with depth below junction when high implantation energies (such as 60 keV and 150 keV) are used, while the concentration and depth below junction have an inverse relationship when low energies (such as 30 keV) are used. On the other hand, the defect concentration increases with increase in implant energy for all samples and all depths. It is also apparent that high implant energy or greater acceleration voltages for the implants cause more damage in the deeper regions of the sample while damage cause by low implant energy is much smaller in that region.

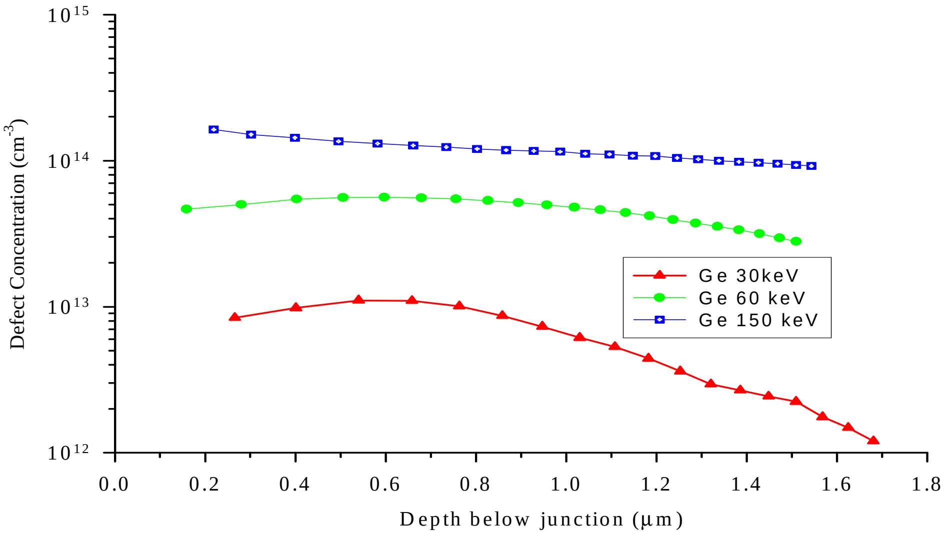

Fig 4: Defect concentration against depth below the junction for samples P16, P10 and P06. Effectively, low implant energies mainly generates shallow level defects. On the other hand, high implant energies generate both shall and deep level defects and in both cases ate relatively higher proportions compared to low energies.

4. CONCLUSIONs

The ion-implantation process was shown to induce defects whose concentration increased as with increase in the applied the Ge implant energy. The defect E(0.42) can only be associated with Ge implantation asit is not observed in reference sample P21. Intensity or peaks and defect concentration increase with increase in implantation energy. The investigation also revealed a proportional relationship between current density and defect concentration due to the fact that more defects lead to amplification of leakage current. The regard to defect concentration at different depths, it can be concluded that, high implant energy cause more damage in the deeper regions of the sample. In terms of character, the defects formed were largely end of range dislocation loops.

5. REFERENCES

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