***Original Research Article***

# Challenges and Resolution for Copper Wirebonding on Tapeless Leadframe Chip-On-Lead Technology


## ABSTRACT

This technical paper discusses a methodological and systematic way of resolving key challenges during introduction of Chip-On-Lead package specifically wirebonding issues that leads to production dilemma during production ramp-up of products using copper wire in tapeless leadframe. The project was intended to determine the "Red-X" or the major cause of yield detractors that may lead to quality issue during wirebonding process.

Problem solving tools were showcased in this paper such as Data Analysis, Cause and Effect, Design-of–Experiment (DOE) and mechanical dimensional analysis which provided substantial impact in determining the real root-cause of the problem. Step-by-step elimination of variables was achieved with the use of statistical engineering tools. Outcome of the project eliminated the occurrence of Non-Stick-On-Pad (NSOP) during wirebonding process without cost involved and just optimizing the available in-house resources. The improvements also enhanced the quality of the product after final test which on the other hand lower the risk of having potential customer complaint in the future.



*Keywords: Chip-on-lead; tapeless leadframe; copper wirebonding; non-stick-on-pad*


## 1. INTRODUCTION

In order to survive the fast-paced changing technology in Semiconductor Industry, we should be flexible in adapting to change to have a very good impression from the customer, would it be internal or external. This is one of the biggest challenges for any semiconductor company in order to maintain its competitive market position and value. However, failure to provide customer expectation will result to possible business failure.

The development of Copper (Cu) wire is the biggest leap today on the semiconductor industry providing cost efficient and high power devices [1] [2] [3]. Copper wire provides better conductivity than Gold (Au) and Aluminum (Al), in which helps offer a better heat dissipation and increased power ratings even with thinner wire application. Another outstanding characteristics of Copper compared to Gold is its mechanical properties, it demonstrate excellent ball to neck strength and high loop stability during encapsulation process. The integration of copper wire technology has been a big challenge in semiconductor manufacturing. This new technology has provided manufacturability apprehensions at wirebond process, specifically on the latest portfolio of Chip-On-Lead (COL) tapeless leadframe-based packages. With the introduction of Copper, Chip-On-Lead package, and the tapeless leadframe, wirebonding process becomes complicated and more challenging.

During production ramp up stage, wirebond performance yield of the package or device in focus (hereinafter referred to as Device C) is unacceptable, averaging only 96% with Non-

Stick-On-Pad (NSOP) during wirebonding as top defect contributor. The plant needs to impress the leading Customer in terms of Delivery requirements without sacrificing the Quality, thus any quality issues especially at Wirebonding which greatly affects electrical performance of the product needs to be addressed. With the continuing technology trends and state-of-the-art platforms [4] [5], this technical paper will discuss how the burden was turned into milestones when top yield detractors of critical processes were addressed by in depth engineering analysis and utilizing statistical tools at early stage of production.

## 1.1 Chip-On-Lead Package Construction

Chip-On-Lead (COL) is a technology where die or crystal is mounted on the leads of the leadframe instead of the paddle. To make it complicated, this leadframe has no tape for support during wirebonding unlike conventional leadframe.

Chip-On-Lead packages have not only provided a low cost solution on reducing body size requirements, but also have shown proven package robustness meeting target reliability performances and key quality and productivity indices that enabled a production worthy package.

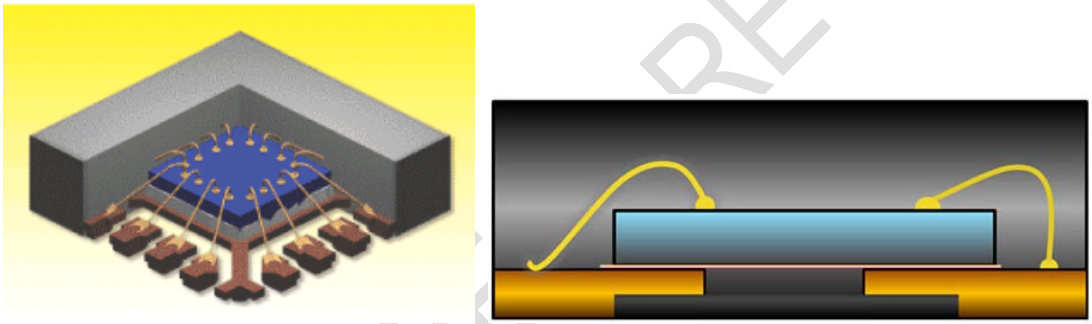


**Fig. 1. 3D view of Quad Flat No-leads (QFN) package and cross-section view**

**Fig. 2. Typical molded package outline**

## 1.2 Copper Wire in Thermosonic Wirebonding

Wirebonding is the process of providing electrical connection between the silicon chip and the external leads of the semiconductor device using very fine bonding wires. The wire used in wirebonding is usually made either of gold (Au) or aluminum (Al), although copper (Cu) wires are starting to gain attention in the semiconductor manufacturing industry. There are two common wirebond processes: ball bonding and wedge bonding.

In the case of Device C, Copper (Cu) and ball bonding is being used. During ball bonding, a ball is first formed by melting the end of the wire (which is held by a bonding tool known as a capillary) through electronic flame-off (EFO). This free-air ball has a diameter ranging from

1.5 to 2.5 times the wire diameter. Free air ball size consistency, controlled by the EFO and the tail length, is critical in good bonding. The free-air ball is then brought into contact with the bond pad. Adequate amounts of pressure, heat, and ultrasonic forces are then applied to the ball for a specific amount of time, forming the initial metallurgical weld between the ball and the bond pad as well as deforming the ball bond itself into its final shape. The wire is then run to the corresponding finger of the leadframe, forming a gradual arc or "loop" between the bond pad and the lead finger. Pressure and ultrasonic forces are applied to the wire to form the second bond (known as a wedge bond, stitch bond, or fishtail bond) this time with the lead finger. The wire bonding machine or wire bonder breaks the wire in preparation for the next wire bond cycle by clamping the wire and raising the capillary.


**Fig. 3. Wirebonding process mechanism**

## 1.3 The Chip-On-Lead Tapeless Leadframe

Tapeless Chip-On-Lead Package is a leadframe-based package carrier (platform) in which the leads footprint will be formed by back-etching process. The plant has a lot to gain with Tapeless Package - Cheaper leadframe cost, Copper wire compatible, no tape and faster sawing speed in Singulation. At the onset of the introduction, one process revealed as most critical and encountered a lot of challenges, this is Copper Wirebonding.

## 1.4 Cost Impact of Copper Wire and Its Performance

The device technology trend continues to become critical and complex. Just recently, ST Calamba launched the very first product that uses copper in wirebonding and tapeless leadframe for Chip-On-Lead package. We all know that price of copper is 75% cheaper than gold and once materialized will bring a lot of savings and will create more business in the company. But like any other new products, this product faced a lot of challenges that later on transformed into milestones.

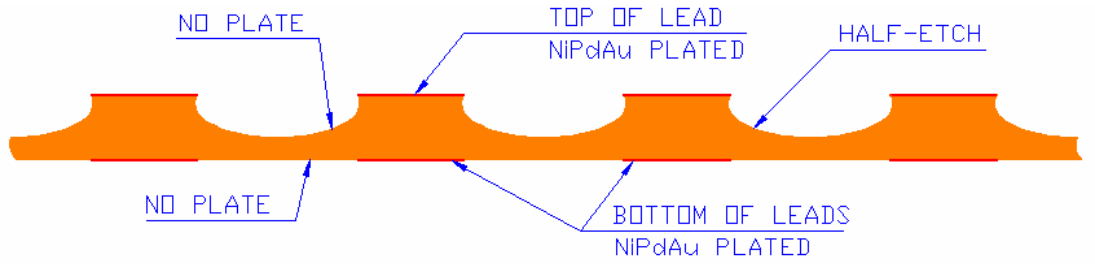



**Fig. 4. Tapeless leadframe configuration**

Aside from being cost efficient, Copper has several advantages over Gold. First, copper (resistivity = 17.24 Ω-m) has a lower resistivity compared to gold (resistivity = 23.26 Ω-m) which leads to move signals faster. Copper helps improve increased device power ratings even with thinner wire application. Furthermore, the electrical conductivity (reciprocal of resistivity) is a major advantage of copper over gold; in fact it is 25% better. Electrical conductivity of Copper is $5.8 \times 10^7$ Siemens/m while Gold is at $4.3 \times 10^7$ Siemens/m. In line with this copper wire can be used for higher performance of fine pitch applications (smaller pad sizes), power management devices and increases operating current of the device. The third major advantage of Copper wire is its thermal conductance. Copper has 39.5 kW/m² K compared to Gold of 31.1 kW/m² K. Some of the benefits of this characteristic is better heat dissipation in package, low risk of recrystallization when heat is applied and low loop applications. Lastly, one of the major differences of Copper versus Gold is in its intermetallic growth Gold intermetallic growth significantly increased over time, which makes the bonding interface brittle. On the other hand, copper have lower IMC growth which increases bonding strength. Slower IMC growth also helps improved device reliability and performance because of lower electrical resistance and lower heat generation.

## 1.5 Device in Focus

Device C is an Electrically Erasable Programmable Read-Only Memory (EEPROM) device with CMOSF8HP4 Die technology and packaged in a tapeless leadframe configuration. The package thickness is at 0.55 mm, with only 5 leads or pins. Shown in Fig. 5 is the device configuration.


**Fig. 5. Device C configuration**

## 1.6 Full Process Flow

During initial phase of the investigation, all possible variables to determine the yield loss contributors were studied. In the case of Device C, the entire processes were analyzed as

this product carries a new process bricks and technology in Calamba such as use of copper at wirebonding and tapeless leadframe which is more sensitive than the conventional leadframe. Bar Graph below showed the yield loss contribution per process and their corresponding rejection rate as source of yield loss during ramp up stage. Fig. 6 shows the assembly process flow. It is worth noting that process flow varies with the product and the technology [6] [7] [8].

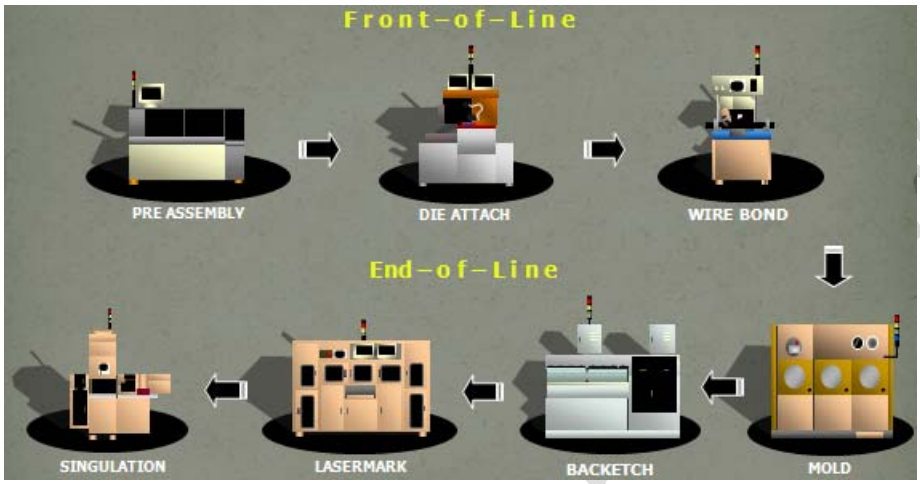



**Fig. 6. Device C assembly process flow**

During the investigation, it was established that the major source of yield loss during ramp up stage is Wirebond. This is a substantial finding so that attention and effort for the root-cause analysis will only focus on this process. Furthermore, yield detractors and top defects were also identified by collecting defect signatures that will serve as lead to further investigate and analyze the root-cause of the problems.

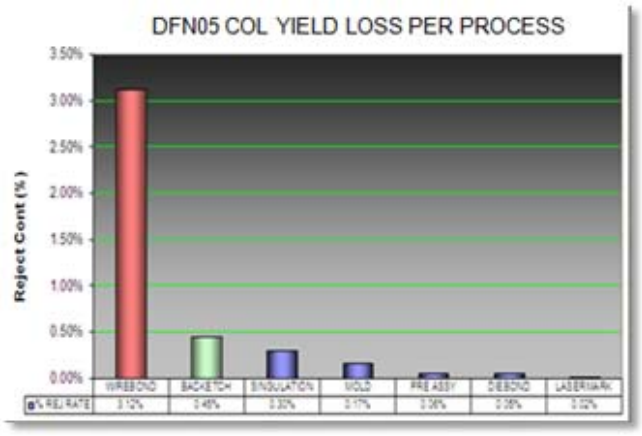



**Fig. 7. Pareto diagram of yield loss contributor per process**

Wirebond has ~3.0% yield loss and considered as HIGH priority among other assembly processes. Furthermore, Problem Definition Tree was established, a structured step-by-step statistical tool used in the analysis to systematically guide the team and identify the top

priority. Shown below is the Project Definition Tree (PDT) where all factors affecting the Device C low yield were considered and comprehended.

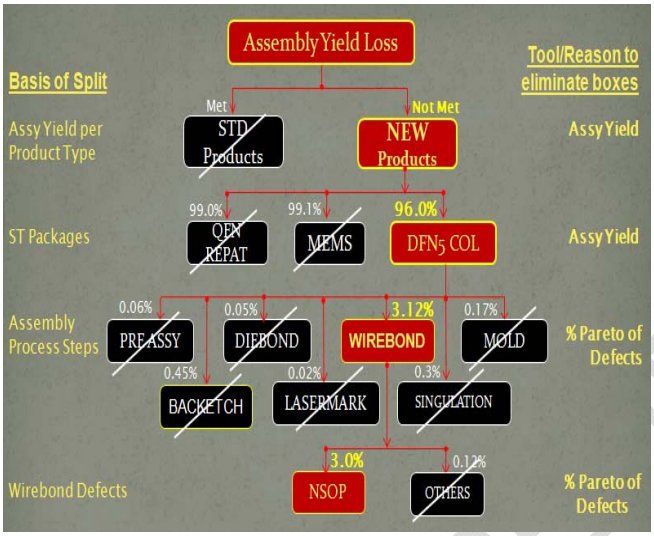



**Fig. 8. Problem definition tree**

Likewise, in order to have a lead on the problems for each process, the team talked to the parts as actual defects were collected, studied and analyze deeper based on defect signatures.

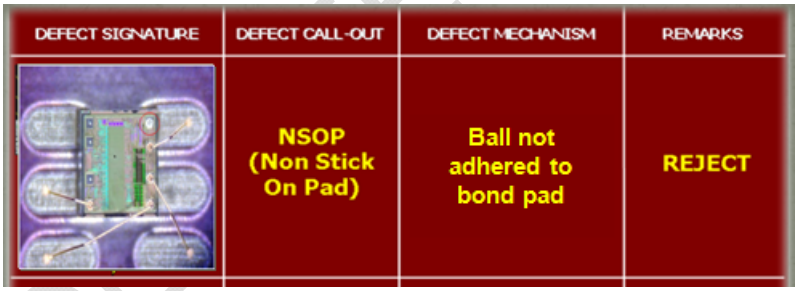



**Fig. 9. NSOP wirebond defect characterization**

Several lots (as shown above) during ramp-up in production was severely affected and way above the allowable PPM level of 0.5%.

## 1.7 Problem Statement

NSOP with an average of 3.0% rejection rate per lot is classified as Wirebonding related defects provide significant failure that substantially affects the Assembly yield with only ~96% during ramp up stage of Device C.

Majority of the process batches were put on-hold and visually inspected due to alarming high rejection rate not meeting the 0.5% NSOP baseline criteria. Batches having NSOP >0.5% were evident per lot during ramp up.

## 2. EXPERIMENTAL SECTION

### 2.1 Root-Cause Analysis: Fishbone Analysis

To capture all variables or potential causes leading to NSOP, Fishbone Diagram in Fig. 12 and Cause and Effect Diagram in Table 1 were employed. Each causes was validated to come up to the true causes. Below is the table of validations made.

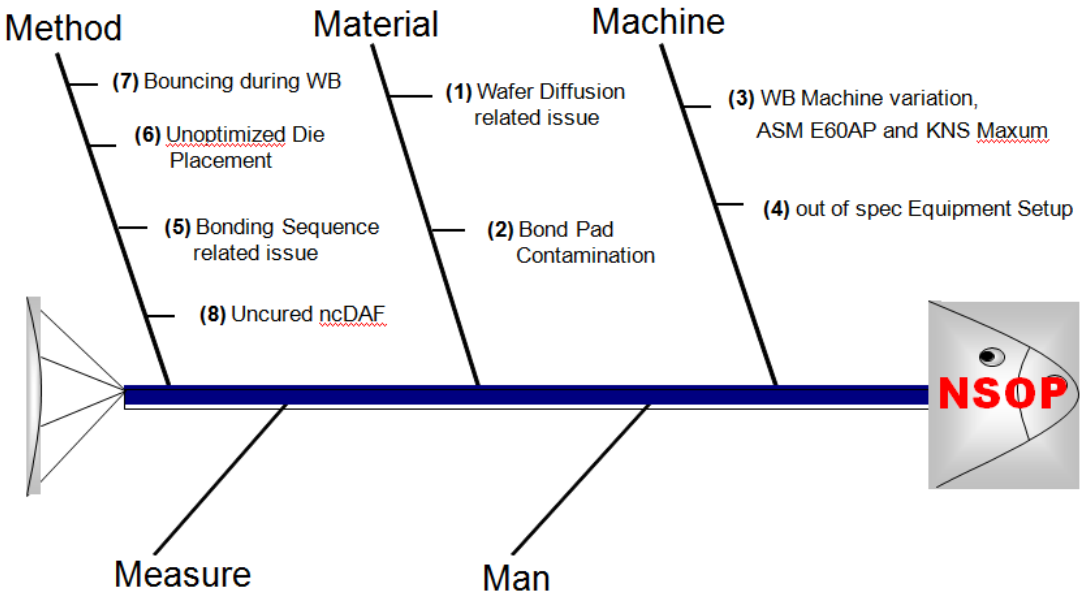



**Fig. 10. Fishbone diagram**

**Table 1. Potential cause validation**

| | Potential Cause | Method of Validation | Result of Validation | Conclusion |
|---|---|---|---|---|
| 1 | Wafer diffusion | Check if problem is isolated on a particular diffusion | All diffusions are affected by NSOP | Not True Cause |
| 2 | Bond pad contamination | Perform EDX analysis on affected pads | No contamination detected | Not True Cause |
| 3 | Wirebond machine variation | Check machine1 and machine2 for NSOP response | Both machines manifest NSOP occurrences | Not True Cause |
| 4 | Out of specification equipment setup | Check equipment parameters for TVC, Air Flow, Vacuum, and Temp | Pertinent parameters within specification | Not True Cause |
| 5 | Bonding sequence related issue | Compare NSOP occurrence when reverse bonding sequence is used | NSOP is encountered at 7/30 units | Not True Cause |
| 6 | Un-optimized die placement | Optimize die placement through DOE | NSOP is encountered at 6/30 units | Not True Cause |

| | | | | |
|---|---|---|---|---|
| 7 | Bouncing during wirebonding | Use high-speed camera to check manifestation of bouncing at pad area during wirebond | Bouncing phenomenon observed: 8/30 NSOP is due to clamp and inserts | True Cause |
| 8 | Uncured ncDAF | Check the DSC of material | ncDAF is fully cured | Not True Cause |

## 2.2 Focusing on NSOP (Non Stick On Pad)

For Wirebond, based on Pareto Principle, the top defect contributor is NSOP (3.0%). The 0.12% OTHERS defect (trivial many – composed of many small percentage of defects) was not included in the analysis to save time and effort.

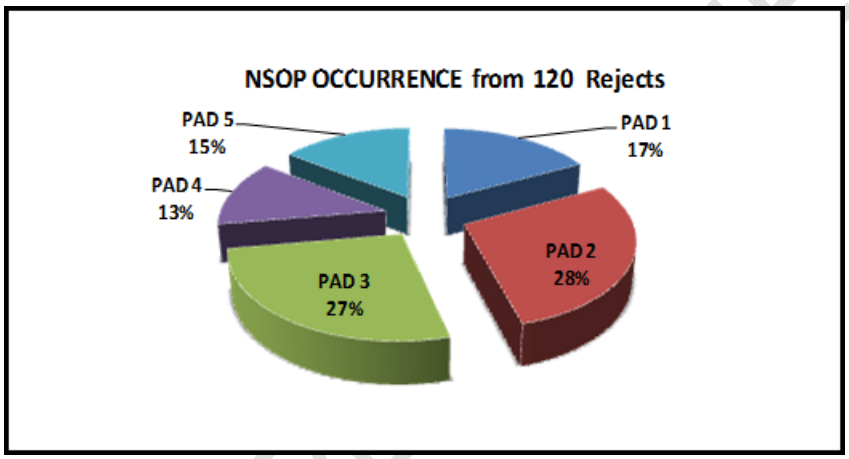



**Fig. 11. NSOP Pie Chart**

Sample photos of bonded units showing NSOP manifestation on pads 1 and 2. Similar manifestation on pads 3, 4 and 5

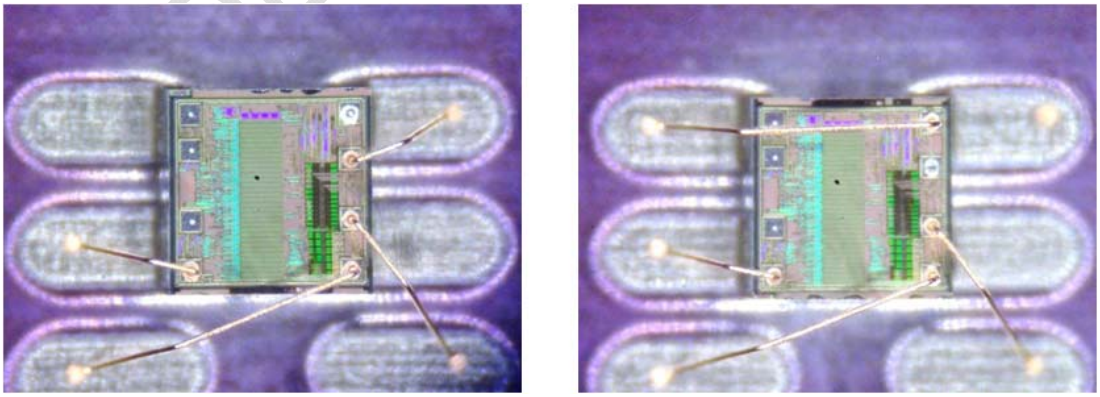


**Fig. 12. NSOP defect mechanism**

Machine-to-machine validation was also performed to check if NSOP defect is not machine related.

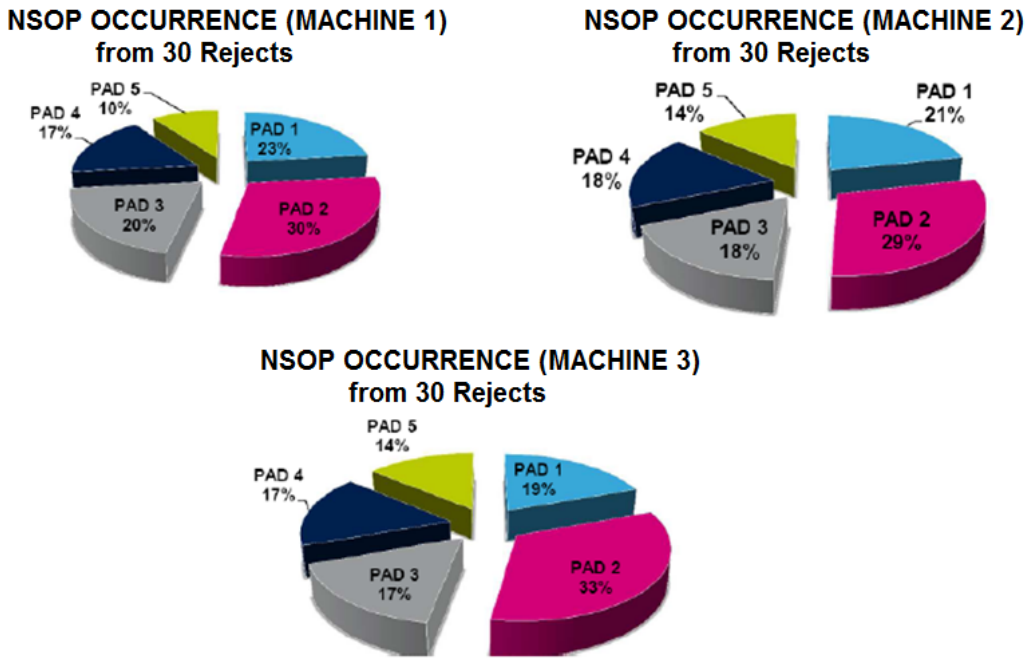



**Fig. 13. Wirebond machine-to-machine comparison**

Table above showed the validation made on all WB machined being used to process Device C. Significant differences in ball shear results. Readings from pads 2 and 3 are passing but are significantly lower than those of pads 1, 4and 5.

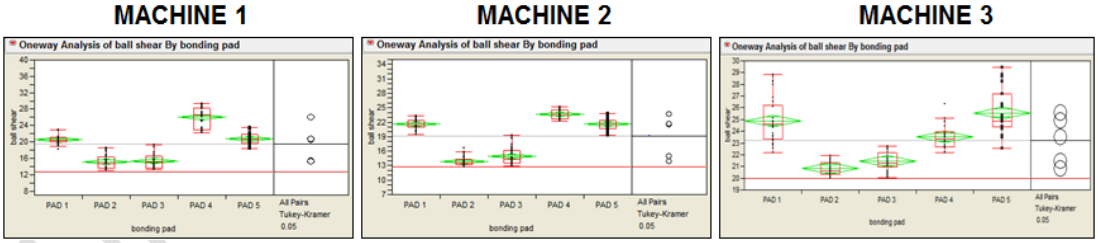



**Fig. 14. Wirebond machines statistical analysis**

The same diffusion wafer batch was splitted into three wirebonding machines but gave the same results and level of NSOP rejects. So WB machine was set aside in the investigation.

## 2.2 Why-Why Analysis

Digging deeper, further validation was made through WHY-WHY analysis. This confirms that the “RED X” is the configuration of the designed insert used during the line stressing lot of Device C, this is causing the NSOP rejection.

**Table 2. Technical root-cause why-why analysis**

| Why 1 | Why 2 | Why 3 | Why 4 | Why 5 | Why 6 |
|---|---|---|---|---|---|
| Bouncing on leadframe pad area during wirebond resulting to NSOP | Leadframe pad area is not firmly hold upon vacuum activation after panel clamping | Presence of entrapped air between leadframe and insert | Air is not able to escape through the designed holes in the insert | Vacuum holes are located too far apart (not fit for Device B density) | It is the configuration of the designed insert used for the affected 2nd line stressing lot of Device B |

More holes on the insert avoid air traps in between units and eventually flatten the lead frame during vacuum at WB.

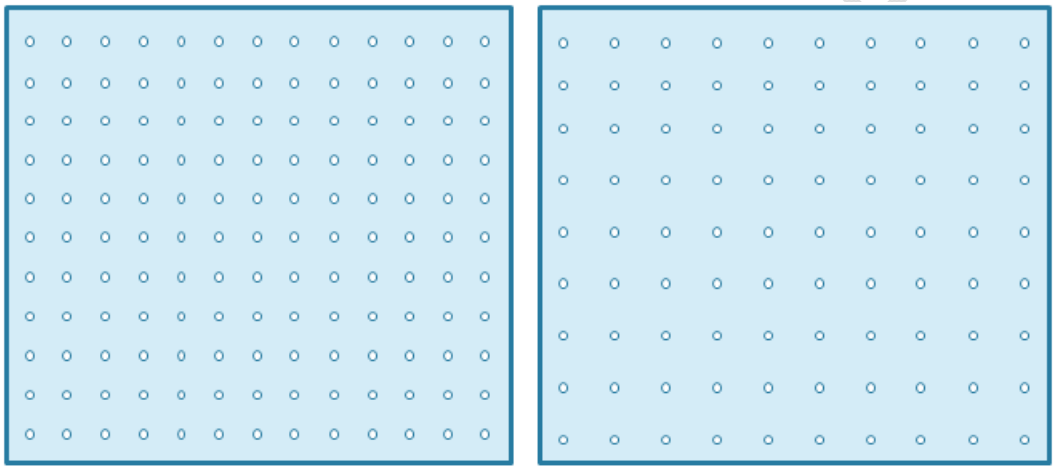



**Fig. 15.** Old and new inserts comparison

A flattened leadframe results to better wirebond quality and less probability of NSOP occurrence.

**Table 3. Systematic root-cause why-why analysis**

| Why 1 | Why 2 | Why 3 | Why 4 | Why 5 |
|---|---|---|---|---|
| It is the configuration of the new insert used for the affected 2nd line stressing lot | The configuration of the insert was designed by the supplier based on the LF drawing provided (in reference to the requested design change for the window clamp | As per current practice for clamp and insert design for new products | | |

| | | | |
|---|---|---|---|
| of Device B | The change in insert configuration (from qualification to line stressing) was not detected upon delivery and use<br><br>Focus is on the requested change in clam window opening | No incoming buy-off or inspection done for the new clamp and insert | Buy-off of clamp and insert not part of the procedure<br><br>Only functional buy-off is done (on actual unit processing) |

**Table 4. Escape root-cause why-why analysis**

| Why 1 | Why 2 | Why 3 | Why 4 | Why 5 |
|---|---|---|---|---|
| Not Applicable<br>NSOP was effectively detected by the current control (alarm) during wirebond | | | | |

## 3. RESULTS AND DISCUSSION

Results of comprehensive investigation thru fishbone and Why-why analysis showed that the root-cause of HIGH NSOP Rejection rate can be attributed to Clamp and Insert design, most particularly the Insert Design. This was identified after series of analysis and validation using different runs. The results was further strengthened by using a high speed camera that helped pinpoint the rootcause of the NSOP phenomena. Results revealed that by using the modified insert design with more holes will address NSOP rejection without sacrificing quality requirements of the products including reliability.

### 3.1 New Clamp and Insert Design

A DOE for 1st bond parameters was conducted with the objective to determine and define window that will minimize occurrence of NSOP. Shown below is the DOE matrix ran using SAS-JMP [9], a system software calculates automatically the combination of runs. New insert design (Rev 1) has total of 1,415 holes to hold 680 units per panel while Original insert design (Rev 0) has only 220 holes.

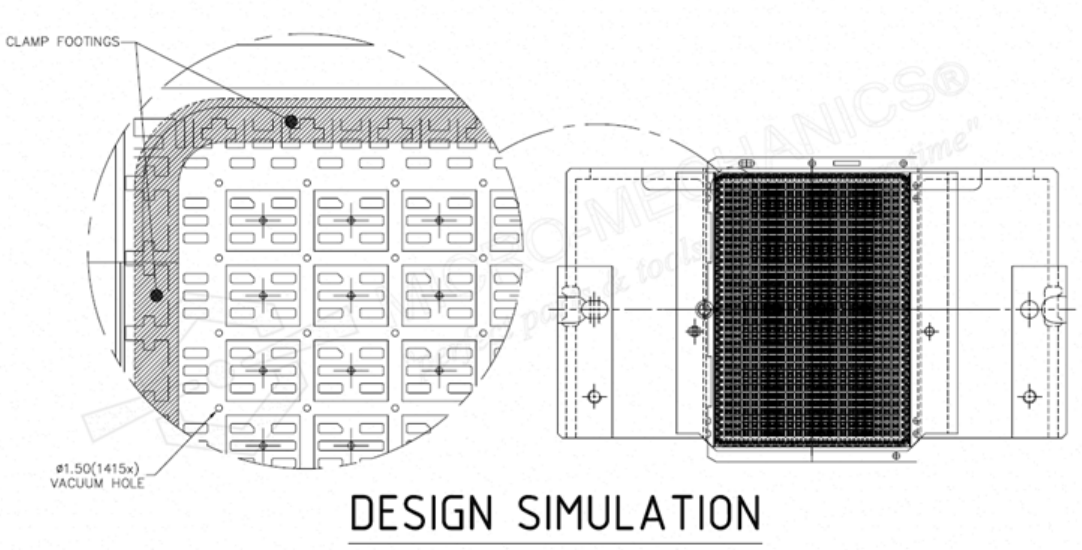



**Fig. 16.** New design of clamp and inserts

T-Test / Analysis of Variance revealed significant difference using New Design/parameters.

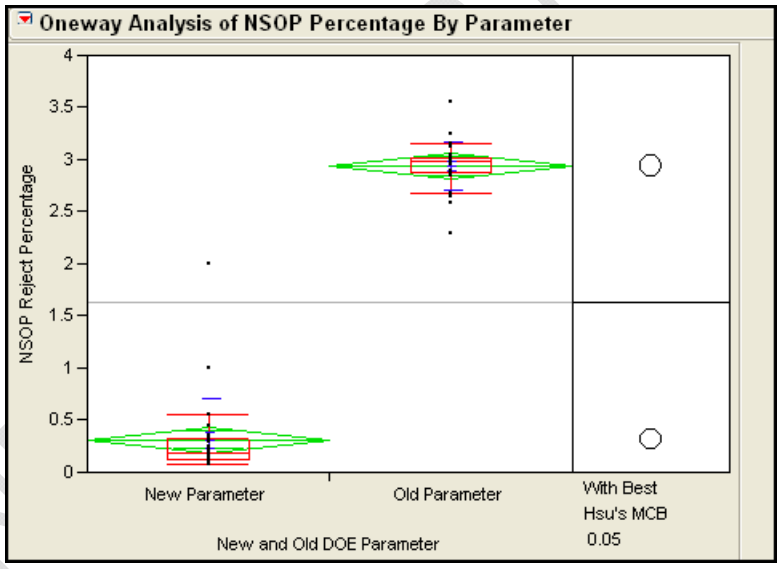



**Fig. 17.** Statistical analysis graph showing significant difference between parameters on old and new clamp and insert design in terms of NSOP attribute data

## 3.2 On-Off Validations

To strengthen the premise on NSOP is due to Clamp and Insert design. Wirebond parameters were brought back to its original set-up. Employing ON-OFF validation, it was very clear that new Clamp and Insert dictates the outcome of NSOP rejection rate. Results of all experiments and validation runs strengthen the conclusion that the NSOP due to poor

design of clamp and insert can be mitigated using higher new design with enhanced vacuum capability.

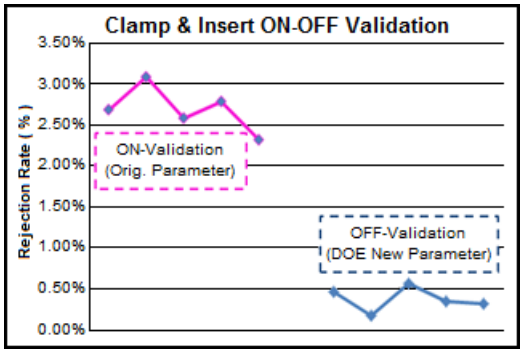



**Fig. 18.** Clamp and insert design/parameters On-Off validation

### 3.3 Response on Critical Product Characteristics

To further verify if the new set of parameters will satisfy the quality requirements based on ST standards, critical responses were studied and collected. Below are the results.

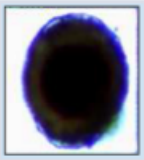
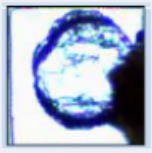
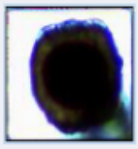
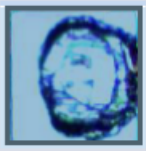
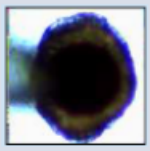
| Parameter | Ball Shear | Wirepull | Remarks |
|---|---|---|---|
| LOW SIDE (LL) |  |  | PASSED Quality Requirements |
| NOMINAL (MID) |  |  | PASSED Quality Requirements |
| HIGH SIDE (HH) |  |  | PASSED Quality Requirements |

**Fig. 19.** Ball shear and wire pull test results

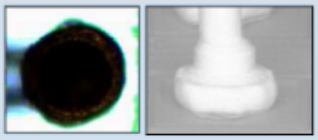
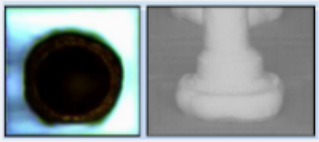
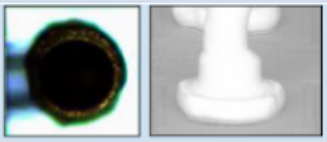
| Parameter | Ball Profile | Remarks |
|---|---|---|
| LOW SIDE (LL) |  | PASSED Quality Requirements |
| NOMINAL (MID) |  | PASSED Quality Requirements |
| HIGH SIDE (HH) |  | PASSED Quality Requirements |

**Fig. 20.** Ball profile results

| Parameter | Cratering | Remarks |
|---|---|---|
| LOW SIDE (LL) |  | PASSED Quality Requirements :NO bond pad damage observed |
| NOMINAL (MID) |  | PASSED Quality Requirements :NO bond pad damage observed |
| HIGH SIDE (HH) |  | PASSED Quality Requirements :NO bond pad damage observed |

**Fig. 21.** Cratering results

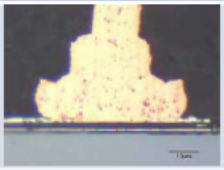
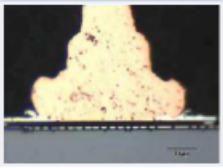
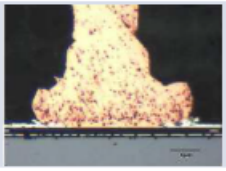
| Parameter | Cross Section | Remarks |
|---|---|---|
| LOW SIDE (LL) |  | PASSED Quality Requirements : Fully ball bond flatness |
| NOMINAL (MID) |  | PASSED Quality Requirements : Fully ball bond flatness |
| HIGH SIDE (HH) |  | PASSED Quality Requirements : Fully ball bond flatness |

**Fig. 22.** Cratering results

### 3.4 Solution Implementation and Mass Production

After replacement of new Clamp and Insert design that mitigates the risk of NSOP defects and validations in terms of Quality and Reliability aspects, large scale evaluations were made through Line Stressing to validate effectiveness of new Clamp and Insert design. Error proofing was employed to identify actions that will either control or eliminate these errors.

Continuous monitoring on the lots during mass production was carried out. Result of verification, Lot using new Clamp and Insert design has an average of 0.32% reject rate.

NSOP trending together with the action and date of execution was monitor to confirmed and validate the effectiveness of the implemented solution. Shown above is the detailed monitoring graph regarding NSOP before and after the solution implementation.

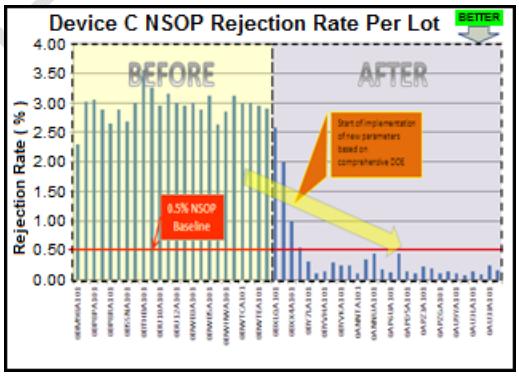



**Fig. 23.** NSOP lot trend before and after the implementation of the corrective actions

Other factors were also measured particularly scrapping of lots due to high NSOP rejection. Succeeding graphs will show the positive impact after the implementation of corrective action.

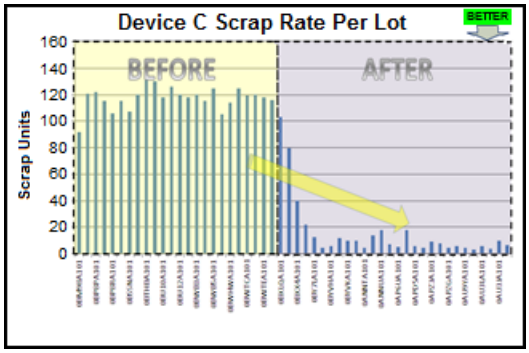



**Fig. 24.** Scrap rate improved after implementation of corrective actions

Significant effect was felt in Scrap rate and increasing Assembly Yield by more than 3% and meeting the WB yield of 99.5%. Yield trend become stable after the implementation of corrective action.

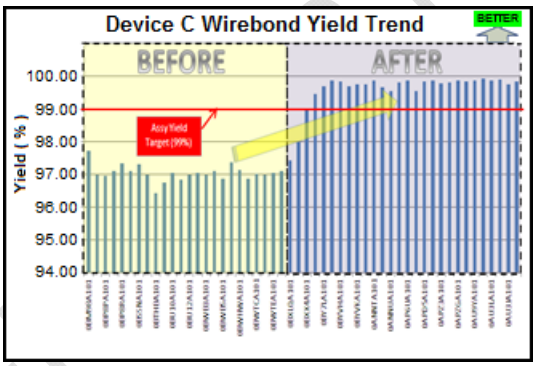



**Fig. 25.** Assembly wirebond yield trend

## 4. CONCLUSIONS AND RECOMMENDATIONS

In depth methodological analysis and statistical techniques for solving the NSOP defects were presented on this paper. Using the knowledge and understanding on data and defect phenomena lead us to pinpoint the true cause of this defect. Comprehensive Why-Why Analysis and Validation mitigates the NSOP rejects which are attributed to design of insert used during qualification affecting the performance Cu wirebonding of Device C package. By changing the design of the Clamp and Insert occurrence of NSOP rejects as manifested during line stressing and validation of run. NSOP defect was solved without too much cost involved and no major modification on the assembly process.

It is recommended that the corrective actions identified, be fanned out to other on-going package development and update the pertinent procedure to include the Clamp and Insert

Design Review with suppliers and internal stakeholders, and corresponding Buyoff Procedure.

It is also highly recommended, if not necessary, that the assembly manufacturing processes observe proper ESD controls. Opportunities presented in [10] [11] could be very useful to help ensure ESD check and controls. Ultimately, continuous improvement is important for sustaining the quality excellence of any product and of the assembly plant.

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