

REVISED V2 A Novel Multiplier using Vedic Mathematics 3 and Booth Encoding

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A Novel Multiplier using Vedic Mathematics and Booth Encoding

SAMPLE ABSTRACT:

In this paper a comparative study of multiplier is done for speed. The concept used in the proposed algorithm is the combination of "UrdhvaTiryagbhyam" algorithm and Booth encoding for performing multiplication. The "UrdhvaTiryagbhyam" algorithm is an ancient Indian Vedic mathematics, which is used for multiplication to improve the speed and area [1]. The multipliers based on the concept of Booth encoding are compact and have significantly a higher speed when compared to their non encoded counterparts [6].

The approached architecture for a multiplier uses Booth encoder, Vedic Multiplier, along with parallel adders. The coding for the proposed multiplier is carried out using the hardware descriptive language namely VHDL. Subsequently the code is simulated and synthesized using Xilinx ISE 10.1 software. This multiplier is implemented on Spartan 3 FPGA devices XC3S50- 5pq208. The performance metrics for comparing the Booth encoded multiplier and the Vedic multiplier is the speed of operation and the device utilization summary, when both the algorithms are implemented on FPGA. It has been observed that the proposed design has speed improvements as compared to the other multipliers.

Keywords: Vedic Multiplier, Booth Encoding, Multiplier, Multiplication, VHDL, FPGA, Synthesis

1. INTRODUCTION

Many digital signals processing operation requires several multiplication and for the same, we need very fast multiplier for a wide range of requirements for hardware and speed. Vedic mathematics was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). The Multiplier Architecture is based on the Vertical and Crosswise algorithm of ancient Indian Vedic Mathematics. Vedic mathematics simplifies and optimizes the conventional mathematical algorithm.

For serial multiplication, Booth encoding based multipliers was proposed. In this method, the partial products are generated by choosing a pair of digits along with the most significant digit from the preceding pair. The multiplier is encoded using radix-2 or radix-4 Booth algorithm [2]. The advantage of Booth encoding is that it generates only half of the partial products in comparison to the other multipliers. However the benefit comes from speed hardware trade off.

We have developed a new architecture using "Urdhva Tiryagbhyam" Sutra and Booth encoding. The final parallel adders implemented in the proposed architecture reduce propagation delay significantly. It is believed that our architecture may set new path for future research.

An organization of this paper is as: section 2 describes the Vedic multiplier using "Urdhva Tiryagbhyam" sutra. Section 3 describes the multiplier using Booth Encoding algorithm. Section 4 shows proposed architecture using carry save adders for 4 bit multipliers. Section 5 describes results, comparison with the Booth encoded multiplier and Vedic multiplier. Conclusion and references are given in section 6 and 7 respectively.

2. VEDIC MULTIPLIER USING 'URDHVA TIRYAGBHYAM'SUTRA.

The "Urdhva Tiryagbhyam" Sutra [1] is a general multiplication formula applicable to all cases multiplication. "Urdhva" and "Tiryagbhyam" words are derived from Sanskrit literature. "Urdhva" means "Vertically" and "Tiryagbhyam" means crosswise.

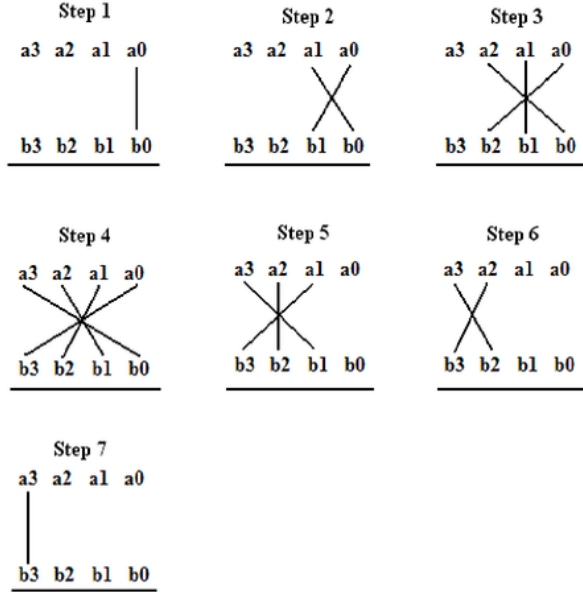


Figure 1: Line Diagram for multiplication of two 4-bit numbers

To illustrate the multiplication algorithm for bit 10, let us consider a multiplication of two binary numbers $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$. The parallelism in generation of partial products and their summation is explained in Figure 1.

3. BOOTH ENCODING

In array multipliers, the computation of the partial products is based on considering one bit of the multiplier at a time. An n -bit by n -bit array multiplier requires ' n ' half adders and ' $n(n-2)$ ' full adders. Hence it can be observed that the number of adders have increased quadratically with an increase in the size of the multiplier.

Booth encoding method was proposed to expedite the serial multiplication. In this method, the Partial products are generated by considering a pair of digits along with the most significant digit from the preceding pair. The multiplier represented as (X) is decoded into distinct select lines and driven across the row, where partial products are generated. These select lines control Booth selectors that choose the appropriate multiple of Y for each partial product. In case of negative numbers, the negative partial products are sign extended in order to be summed precisely. The Booth encoded multipliers are compact and faster compared to the other popular multipliers [6].

Y is the multiplicand and X is the multiplier. Every Addition/Subtraction/NOP is followed by right shift by 2 bits.

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TABLE 1: Radix-4 Booth Encoding.

Multiplier (X)	Encoding	Action to be taken
000	0	NOP
001	+1	Add Y
010	+1	Add Y
011	+2	Add Y twice
100	-2	Add 2s complement of Y two times
101	-1	Add 1s complement of Y
110	-1	Add 1s complement of Y
111	0	NOP

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98 The motivation for this work was obtained by making a survey of fast multipliers that could
99 be used in encryption algorithms. In the survey, many authors have compared the Booth
100 Multiplier with the Vedic Multiplier. It has been observed from the Survey that the delay of
101 Vedic multiplier was 20% reduced in comparison to the Booth Encoded Multiplier.
102 Also in an NXN Vedic multiplier, 'n' bits of the multiplier are considered for generating the
103 partial product. But since, Parallelism is involved in the generation of the partial products.
104 Vedic multiplier is found to have a lower delay.

105 Whereas in an NXN Booth encoded multiplier, only 'n/2' bits of the multiplier are
106 considered for generating the partial product. But the partial products are generated
107 serially.

108 In the proposed algorithm, the multiplier is encoded using Booth encoding, in order to
109 reduce the number of multiplier bits to 'n/2'. In addition to this, Parallelism is also involved
110 in the generation of the partial products. Hence the benefits of the Vedic multiplier and that
111 of the Booth encoder are combined together in order to further reduce the delay.

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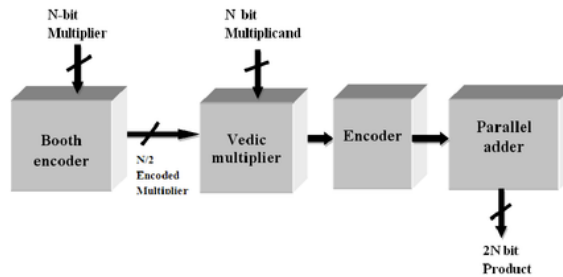
4. PROPOSED ARCHITECTURE

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114 Figure 2 shows the proposed architecture for multiplication of N bit binary number
115 using Booth encoding and Vedic mathematics.

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117 In the proposed architecture the N bit multiplier is encoded into a N/2 bit multiplier
118 using radix 4 Booth encoding. To illustrate with an example, let us consider 4 bit
119 multiplication:
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Figure-2: Proposed Architecture

The multiplicand X is represented as X3 X2 X1 X0 and the multiplier Y is represented Y3 Y2 Y1 Y0. By applying the Booth encoding technique, the multiplier Y gets encoded as YN1 and YN0. With the new encoded multiplier all the partial products are computed parallelly using the Vedic multiplier. After the application of "Urdhva Tiryakbhyam" Sutra and Booth encoding the partial products obtained are

$$\begin{aligned} P0 &= X0 YN0 \\ P1 &= X1 YN0 \\ P2 &= X2 YN0 + X0 YN1 \\ P3 &= X3 YN0 + X1 YN1 \\ P4 &= X2 YN1 \\ P5 &= X3 YN1 \end{aligned}$$

The encoding of the partial products after the application of both the algorithms is discussed in Table -2.

TABLE -2 : Encoded Values

Partial Products (P5 to P0)	Encoded Values (PE)
0	0000
1	0001
2	0010
3	0011
4	0100
-4	1100
-3	1101
-2	1110
-1	1111

The encoded values for each of the partial products P5 to P0 are PE5 PE4 PE3 PE2 PE1 PE0. Figure 3 and 4 shows the final product obtained after the encoded values are shifted and fed to the Parallel adder.

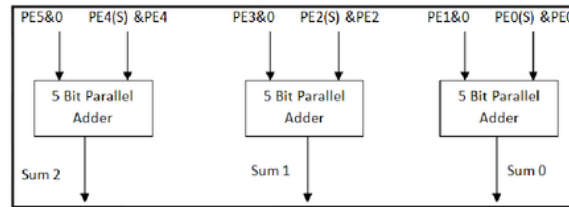
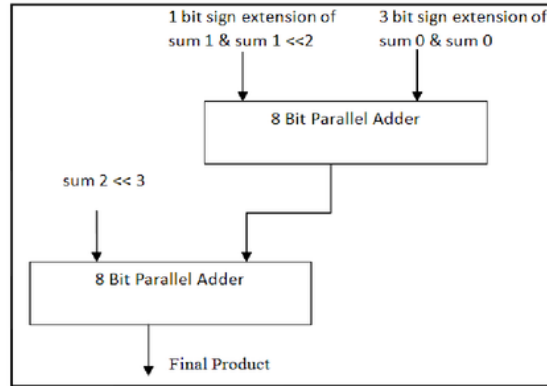


Figure-3 : Parallel addition of encoded values.

From Figure 3, it is shown that PE0, PE2 and PE4 are sign extended by one bit. Whereas PE1, PE3 and PE5 are left shifted by one bit position before applying to the 5 bit parallel adder. Figure-4 shows the final product obtained from the 8bit parallel adder. The 8bit parallel adder takes 3 bit sign extension of Sum0 along with twice left shifted and 1

167 bit sign extension of Sum1. The second stage parallel adder gets its input from the
 168 first stage sum and also thrice left shifted Sum2.
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185 **Figure-4: Addition for Final Product**

186 This proposed architecture reduces the delay considerably compared to both Booth
 187 encoding algorithm [5] and Vedic Mathematics algorithm [3]. The carries generated by the
 188 individual parallel adders are not passed on to the next stage of adders.
 189

190 5. RESULTS AND DISCUSSION

191 Table-3 shows comparison of the proposed architecture with Vedic Mathematics Multiplier [3]
 192 and Booth Encoding Multiplier [5].
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194
195 **TABLE-3: Synthesis Report**

Device Spartan2 XC3S50: 5pq208	4 X 4 Multiplier Using Vedic Mathematics	4 X 4 Multiplier Using Booth Encoding	4 X 4 Multiplier Using proposed Architecture
Delay	17.754 ns	22.209 ns	13.3 ns
Number of Slices	18/768	27/768	38/768
Number of LUTs	33/1536	33/1536	69/1536
Levels of Logic	9	14	7

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199 The proposed architecture for a $N \times N$ multiplier for a value of $N = 4$ is found to
 200 have a delay of 13.3 ns, with 8.168 ns for the logic and 5.132 ns for routing. The
 201 speed is optimized compared to Vedic Mathematics multiplier[3], which has 10.134ns
 202 for logic and 7.632 ns for routing and Booth Encoding Multiplier[5], which has
 203 12.313 ns for logic and 9.896ns for routing, giving a delay reduction of 25% and 40 %
 204 respectively.
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206 Simulation result:

207 The $N \times N$ multiplier, for $N = 4, 8$ designed in VHDL and its functionality is being
 208 verified for all the possible input combination by writing test bench.

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X	0101	0111	1010	0101
Y	1010	0111	1010	
YN0	-2	-1	-2	
YN1	-1	2	-1	
PE0	1110	1111	0000	1110
PE1	0000	1111	1110	0000
PE2	1101	0001	0000	1101
PE3	0000	0010	0001	1101
PE4	1111	0010	0000	1111
PE5	0000	0000	0010	1111
FINALPRODUCT	-30	49	70	-60

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Figure 5. Simulation result for 4 bit proposed multiplier

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Figure 5 shows 4 different values of the operands X and Y.

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The first being $X = (0101)_2 = (5)_d$, $Y = (1010)_2 = (-6)_d$. The operand Y is encoded according to Table 1 as $YN0 = -2$ and $YN1 = -1$. The six partial products generated parallelly are PE0, PE1, PE2, PE3, PE4 and PE5. The final product is $(-30)_d$.

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The second set of operands are $X = (0111)_2 = (7)_d$, $Y = X = (0111)_2 = (7)_d$. This generates the final product as 49. The operand Y is encoded as 2 and -1. The partial products are generated using the Vedic multiplier.

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X	01111111	01111111	11111111	01111111
Y	11111111	01111111	11111111	
YN0	-1	-1		
YN1	0	0		
YN2	0	0		
YN3	0	2	0	
PE0	11111	11111		
PE1	11111	11111		
PE2	11111	11111		
PE3	11111	11111		
PE4	11111	11111		
PE5	11111	11111		
PE6	11111	00001	11111	
PE7	00000	00010	00001	11111
PE8	00000	00010	00000	00000
PE9	00000	00010	00000	00000
PE10	00000	00010	00000	00000
PE11	00000	00010	00000	00000
PE12	00000	00010	00000	00000
PE13	00000	00000	00010	00000
FinalProduct	-127	16129	32385	-255

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Figure 6: Simulation Result for Proposed 8-bit multiplier

Figure 6 shows the ModelSim results for 8 bit proposed multiplier for $X = 11111111$, $Y = 01111111$ yielding a product of 32385 to base 10. The multiplier Y is encoded as 2,0,0,-1 using Booth encoding. The Partial products from PE0 to PE15 (PE14 and PE15 are missing in the figure, due to lack of clarity) are obtained using Vedic multiplier. Similarly for $X = 01111111$, and $Y = 11111111$ the product is -127. In Figures 5 and 6 PEn each is an encoded value. The proposed architecture assumes X to be an unsigned number and Y to be a signed number.

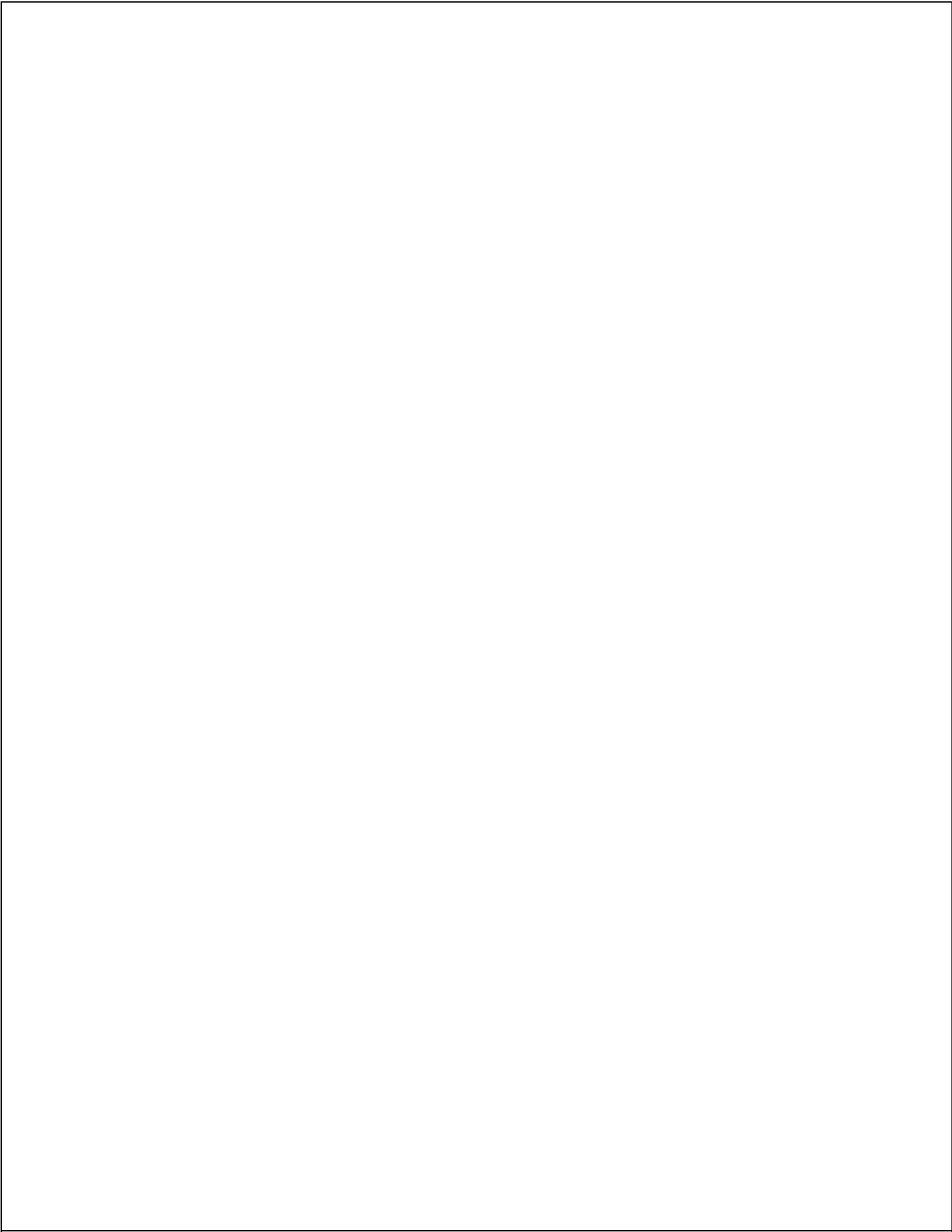
4 CONCLUSIONS

The proposed multiplier architecture which combines the benefits of Booth encoding and the benefits of Vedic multiplier shows speed improvements over multiplier architecture presented in Vedic mathematics [3] and Booth Encoding [5] individually. The $N \times N$ multiplier using the proposed architecture has resulted in delay reduction of 25 % compared to Vedic mathematics and 40% reduction in delay compared to Booth Encoded multiplier. It can be well suited for multiplication of numbers with more than 16 bit size.

This work can be further extended for area optimization and also usage of carry save adders can further reduce the delay.

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