



SDI FINAL EVALUATION FORM 1.1

PART 1:

Journal Name:	Journal of Advances in Mathematics and Computer Science
Manuscript Number:	Ms_JAMCS_37931
Title of the Manuscript:	A Novel Multiplier using Vedic Mathematics and BoothEncoding
Type of Article:	Short research article

PART 2:

FINAL EVALUATOR'S comments on revised paper (if any)	Authors' response to final evaluator's comments
- It is recommended to make it complete yet concise description and explanation. For example, the research question and its relation on proposed solution is not clearly explained in the abstract. - There should be more descriptions on the previous works of related research. This research area is incremental, so it is better to provide a stronger research backgrounds. - In Section-3, Line 92-95, it is said: "The motivation for this work was obtained by comparing the Booth Multiplier with Vedic Multiplier. The delay of Vedic multiplier was 20% reduced compare to Booth Encoded Multiplier. Since Vedic multiplier is faster [4][7], the idea of combining both the methods should further reduce the delay". It is weird, since Vedic is already faster, why do they need to be combined? This reason is also changed from previous writing: "The motivation for this work was obtained by comparing the Booth Multiplier with Vedic Multiplier. The delay of Vedic multiplier was 20% reduced compare to Booth Encoded Multiplier. Since Booth encoding is faster, the idea of combining both the methods should further reduce the delay". Apparently, it has inconsistency. - In Section-4, there is no detailed explanation on how Vedic and Booth techniques combined. It is recommended to described it thoroughly with illustration. - In Section-5, the simulation results should be presented in intuitive ways so the readers can understand the waveform easily. For example, using the decimal number instead of binary. Apparently, it is still the same from before. - This article needs a strong research background and consistency for being accepted.	In this paper a comparative study of multiplier is done for speed. The concept used in the proposed algorithm is the combination of "UrdhvaTiryagbhyam" algorithm and Booth encoding for performing multiplication. The "UrdhvaTiryagbhyam" algorithm is an ancient Indian Vedic mathematics, which is used for multiplication to improve the speed and area [1]. The multipliers based on the concept of Booth encoding are compact and have significantly a higher speed when compared to their non encoded counterparts [6]. These lines have been corrected in the revised paper. Apologies, that in the earlier version, there was a mistake of mentioning delay instead of speed. This mistake has been rectified. Table 1 and the lines after Fig 2, which gives the partial product equations, illustrate the working of the algorithm. The simulation results are explained with an illustration in the new version of the paper.