

A Comparison of the Methods of Boolean-Equation Solving and Input-Domain Constraining for Handling Type-2 Problems of Digital Circuit Design

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ABSTRACT

With the advent of digital computers, several prominent problems of digital circuit design emerged. A particular class of these problems, (called Type-2 problems) can be divided into two subclasses depending on whether an honest translator is possible or a sneaky translator is warranted. The case of an honest translator is simply an inverse problem of logic in which knowledge of the vectorial function $Z(X)$ is utilised to produce its inverse vectorial function $X(Z)$. Though an old method of solving type-2 problems was known almost half a century ago, two modern methods are now possible, namely the method of Boolean-equation solving and the method of input-domain constraining. The purpose of this paper is to expose and illustrate these two novel methods, with a stress on comparing them together and demonstrating their superiority to (as well as agreement with) the old conventional method. This purpose is achieved by way of three typical classical

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examples for which conventional solutions are somewhat tedious and cumbersome, while modern solutions are simple and insightful. Throughout these examples, the Karnaugh map is effectively utilised, either in its conventional version or in its variable-entered version. The Boolean-equation-solving method seems to involve certain unwarranted steps that might be possibly skipped. However, its utility can be extended beyond type-2 problems,

Keywords: 'Big' Boolean algebras; digital circuit design; honest and sneaky translators; type-2 problems.

1. INTRODUCTION

A classical problem of digital circuit design can be described by the general layout of Fig. 1. Various variants or special cases of this layout appeared on early scholarly work on the subject, including the pioneering contributions of Ledley [1, 2], Bell [3], and Brown [4]. Fig. 1 shows a combinational logic circuit C that is comprised of two subnetworks A and B, while the final output can be viewed as output $s(Y, Z)$ or $(s(X, Y, Z))$ of network B or output $t(X, Y)$ of network C. If the shaded path in Fig. 1 can be omitted, network B is called an 'honest translator' [4], while if it is needed (or used), this network is called a 'sneaky translator' [4]. Based on Fig. 1, three 'elementary problems of digital circuit design' are proposed [1-5], which are

Type-1 problem: Given $z(X)$ and $s(X, Y, Z)$, find $t(X, Y)$.

Type-2 problem: Given $z(X)$ and $t(X, Y)$ find $s(Y, Z)$ if an honest translator is possible; otherwise find $s(X, Y, Z)$ for a sneaky translator.

Type-3 problem: Given $s(Y, Z)$ or $s(X, Y, Z)$ as well as $t(X, Y)$, find $z(X)$.

The type-1 problem is solved trivially by direct substitution and does not warrant further attention. The type-2 problem was handled by Ledley [1, 2], Bell [3], and Brown [4]. It has been also treated much more recently (via modern techniques) by Rushdi [5], and will be revised further herein. The type-3 problem has been treated by Ledley [1, 2] and much more recently (via modern techniques) by Rushdi and Ahmad [6].

We now address the probably intriguing question: Why should we bother revisit a problem that was really hot as back as half a century ago. The answer is that new computational methods associated with useful conceptual insight have recently been made possible through a variety of

breakthrough developments made in the past few years. These include:

1. The development of a method to suppress certain variables Y in a parent equation $h(X, Y, Z) = 1$ so as to replace it by a simpler equation $g(X, Z) = 1$ that can be used to solve for Z in terms of X producing the set of solutions $Z(X, Y)$ of the parent equation $h(X, Y, Z)$ that are independent of Y [7].
2. The emergence of a novel method to list all the particular solutions of a 'big' Boolean equation in a very compact space, thereby allowing easy selection of a specific particular solution that enjoys certain desirable features [6, 8, 9].
3. The convenience and power of rewriting interval based conditions of the form $g_l \leq g \leq g_u$ as a don't-care based one $g = g_l \vee d(g_u)$ [11-14].

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Utilising the aforementioned developments, this paper introduces and compares two novel techniques for handling type-2 problems of digital circuit design. These are:

1. A technique using solutions of 'big' Boolean equations. If an honest translator is possible, we are able to handle the inverse problem of logic by using $Z(X)$ to obtain $X(Z)$ and hence produce $t(X, Y) = s(Z(X), Y)$. Otherwise, we produce a sneaky translator $t(X, Z, Y)$. The essence of this technique is quite similar to that used for type-3 problems in [6].
2. A technique that enhances the earlier one of input-domain constraining developed by Brown [4] by augmenting it by the don't-care terminology by Reusch [9], Rushdi [5, 11-13], and Rushdi and Albarakati [14]. This enhancement allows easy minimisation as well as the possibility of handling larger problems via the Variable-Entered Karnaugh Map (VEKM) rather than the Conventional Karnaugh Map (CKM) [5, 11-14].

Details and characteristics of the two novel techniques are clarified herein *via* three detailed examples. Example 1 and 2 were earlier handled by Bell [3], while Example 3 was treated by Ledley [2] and Brown [4] *via* the conventional old method. As we proceed, we will demonstrate advantages of our two competing novel methods compared to the conventional method. These advantages include conceptual clarity, high speed, aggregation of tasks, and better control on outcomes. Such advantages do not pertain only to pedagogical issues but might also be of significant benefit to practical digital design. This introductory section is followed by Sections 2-4 which discuss the aforementioned three design examples. Section 5 discusses our findings while Section 6 concludes the paper.

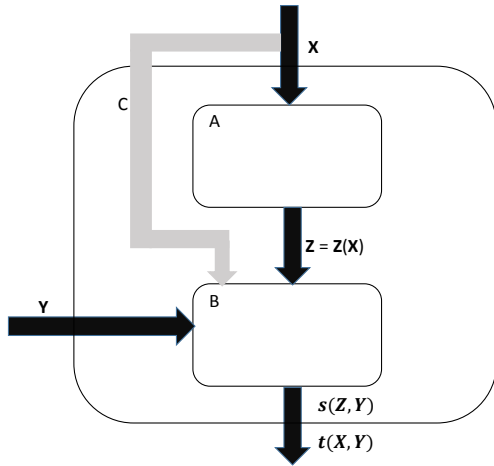


Fig. 1. Layout of a general problem of digital circuit design. If the sneaky (lightly shaded) path is needed or used, the function $s(Z, Y)$ is replaced by $s(X, Z, Y)$

2. A SMALL EXAMPLE CIRCUIT

This example was earlier handled by Bell [3] by the long and old conventional method, and it admits the existence of an honest translator. There are two inputs for subnetwork B (outputs for subnetwork A)

$$Z_1 = X_1 \vee \bar{X}_2, \quad (1)$$

$$Z_2 = X_1 \bar{X}_2, \quad (2)$$

and a single desirable output for the overall network C

$$t(X) = \bar{X}_1 \vee X_2, \quad (3)$$

and there are no side inputs Y for subnetwork B. In our first novel method we obtain $s(Z)$ by first solving an inverse problem of logic (*i.e.*, using $Z(X)$ to derive $X(Z)$) and then obtaining $s(Z)$ *via*

$$s(Z) = t(X(Z)). \quad (4)$$

The information given by $Z(X)$ can be formulated as a single Boolean equation of the form

$$g(X, Z) = (Z_1 \odot (X_1 \vee \bar{X}_2)) (Z_2 \odot (X_1 \bar{X}_2)) = 1. \quad (5)$$

The two-valued Boolean function $g(X, Z): B_2^4 \rightarrow B_2$ is now viewed as a 'big' Boolean function $g(X) = B_{16}^2 \rightarrow B_{16}$, where B_{16} is the free Boolean algebra $FB(Z_1, Z_2)$, so that the roles of Z_1 and Z_2 is switched from that of independent variables to that of generators of B_{16} [14-25]. The natural map for $g(X)$ is shown in Fig. 2. Its entries are some of the 4 atoms of $B_{16} = FB(Z_1, Z_2)$ which are expressed in terms of the generators Z_1 and Z_2 . Since these generators look like "variables" (in fact, they were originally variables), the map is called a Variable-Entered-Karnaugh map (VEKM). We use the technique developed in [15-18] to construct the auxiliary function $G(X, p)$ to be used in deriving the parametric solution of $g(X) = 1$. These solutions are expressed in terms of a single arbitrary parameter $p \in B_2$ as [6, 15, 16, 20]

$$X_1 = Z_1 Z_2 \vee Z_1 \bar{Z}_2 p \vee d(\bar{Z}_1 Z_2), \quad (6a)$$

$$X_2 = \bar{Z}_1 \bar{Z}_2 \vee Z_1 \bar{Z}_2 p \vee d(\bar{Z}_1 Z_2), \quad (6b)$$

$$\bar{X}_1 = \bar{Z}_1 \bar{Z}_2 \vee Z_1 \bar{Z}_2 \bar{p} \vee d(\bar{Z}_1 Z_2), \quad (6c)$$

Substitution of (6b) and (6c) in (3) and (4) results in the following expression

$$\begin{aligned} s(Z) &= \bar{Z}_1 \bar{Z}_2 \vee Z_1 \bar{Z}_2 \bar{p} \vee \bar{Z}_1 \bar{Z}_2 \vee Z_1 \bar{Z}_2 p \vee d(\bar{Z}_1 Z_2) \\ &= \bar{Z}_2 \vee d(\bar{Z}_1), \end{aligned} \quad (7)$$

in which the parameter p disappears. However, depending on whether we nullify or assert the don't-care term in (7), the following two solutions are obtained for $s(Z)$

$$s(Z) = \bar{Z}_2, \quad (8a)$$

or

$$s(Z) = \bar{Z}_2 \vee \bar{Z}_1. \quad (8b)$$

in agreement with the solution obtained in Bell [3].

	X_1		
	$Z_1 \bar{Z}_2$	$Z_1 Z_2$	
	$\bar{Z}_1 \bar{Z}_2$	$Z_1 \bar{Z}_2$	X_2
$g(X)$			

Fig. 2. The natural map for $g(X)$ in Equation (5). Each map entry is a particular minterm or atom over (Z_1, Z_2) . The polarity of Z_1 is positive over $(X_1 \vee \bar{X}_2)$, while that of Z_2 is positive over $X_1 \bar{X}_2$

	X_1		
$Z_1 \bar{Z}_2(\bar{p})$ $\vee d(\bar{Z}_1 Z_2)$	$Z_1 Z_2(1)$ $\vee d(\bar{Z}_1 Z_2)$		
$\bar{Z}_1 \bar{Z}_2(1)$ $\vee d(\bar{Z}_1 Z_2)$	$Z_1 \bar{Z}_2(p)$ $\vee d(\bar{Z}_1 Z_2)$	X_2	
$G(\mathbf{X}, \mathbf{p})$			

Fig. 3. The auxiliary function used to derive the parametric solutions of $g(X) = 1$ in Section 2

Now, we employ our second novel method adapted from the input-domain constraining method of Brown [4]. Our basic information $\mathbf{Z}(X)$ can be cast in the equational form $h(X, \mathbf{Z}) = 0$ where $h(X, \mathbf{Z}) = \bar{g}(X, \mathbf{Z})$ is represented by the natural map for $h(X): B_{16}^2 \rightarrow B_{16}$ in Fig. 4. According to Brown [4], our current problem can be described by

$$\{h = 0\} \Rightarrow \{s = t\}, \quad (9)$$

which has the interval solution

$$\bar{h}t \leq s \leq h \vee t. \quad (10)$$

We now rewrite the double-inequality (10) in the don't-care notation [11-14]

$$\begin{aligned} s &= \bar{h}t \vee d(h \vee t) \\ &= \bar{h}t \vee d(h) \\ &= gt \vee d(\bar{g}). \end{aligned} \quad (11)$$

and use the maps in Figs. 2, 4, and 5 for $\bar{h} = g, h$, and t to construct the natural map for s in Fig. 6 according to (11). This map is simplified by noting that (11) indicates that $s = g \vee d(\bar{g}) = g \vee d(1)$ when $t = 1$, and that $s = d(\bar{g})$ when $t = 0$. Fig. 6 can immediately be used to produce an expression of s that is a function of both X and Z , i.e., a sneaky translator, of the form

$$s(X, \mathbf{Z}) = (\bar{X}_1 \bar{X}_2 \vee X_1 X_2)(Z_1 \bar{Z}_2 \vee d(1)) \vee \bar{X}_1 X_2 (\bar{Z}_1 \bar{Z}_2 \vee d(1)) \vee X_1 \bar{X}_2 d(\bar{Z}_1 \vee \bar{Z}_2). \quad (12)$$

However, we note that none of the four atoms of $FB(Z_1, Z_2)$ has a mixed assertion in the cells of the map of Fig. 6. In fact, each of atoms $Z_1 \bar{Z}_2$ and $\bar{Z}_1 \bar{Z}_2$ is only asserted positively in this map (in cells $\bar{X}_1 \bar{X}_2$ and $X_1 X_2$ for the former atom and cell $\bar{X}_1 X_2$ for the latter one), while the atom $Z_1 Z_2$ is only asserted negatively (in cell $X_1 \bar{X}_2$). By contrast, the atom $Z_1 \bar{Z}_2$ is neither asserted positively or negatively in the map. The lack of any mixed assertion is equivalent to the condition demanded by Brown [4] for an honest translator i.e., one for which s is independent of X [5]. According to the VEKM "enlargement" rule [11, 26, 27], the VEKM in Fig. 6 might be read to yield any of the two solutions in (8). Alternatively, we note that, for an honest translator s is a disjunction of all positively asserted atoms and possibly any of the totally don't-care atoms [5], i.e., s is given by

$$\begin{aligned} s &= Z_1 \bar{Z}_2 \vee \bar{Z}_1 \bar{Z}_2 \vee d(Z_1 Z_2) \\ &= \bar{Z}_2 \vee d(Z_1), \end{aligned} \quad (13)$$

is agreement with (8).

		X_1		
$\bar{Z}_1 \vee Z_2$		$\bar{Z}_1 \vee \bar{Z}_2$		
$Z_1 \vee Z_2$		$\bar{Z}_1 \vee Z_2$		X_2
$h(\mathbf{X}, \mathbf{Z}) = 0$				

Fig. 4. The natural map for $h(X, \mathbf{Z})$ needed in the second method in Section 2

	X_1	
1		
1	1	X_2

$$t(X) = \bar{X}_1 \vee X_2$$

Fig. 5. Conventional Karnaugh map for $t(X)$ expressed by (3) in Section 2

	X_1	
$Z_1 \bar{Z}_2 \vee d(1)$	$d(\bar{Z}_1 \vee \bar{Z}_2)$	X_2
$\bar{Z}_1 \bar{Z}_2 \vee d(1)$	$Z_1 \bar{Z}_2 \vee d(1)$	

$$s(X, Z) = \bar{h}t \vee d(h)$$

Fig. 6. Simplified natural map for $s(X, Z)$ in Section 2

3. AN ASYMMETRIC EXAMPLE CIRCUIT

This example was used by Bell [3] to demonstrate the power of his method and show how it is applied when the number of elements of Z differs from that of X . In the current example, these two numbers are 5 and 4, respectively, while they were 2 and 2 in the example of Section 2. Again, there is no side inputs Y , and $Z(X)$ is given by

$$Z_1(X) = X_1, \quad (14a)$$

$$Z_2(X) = X_1 \bar{X}_4 \vee X_3 X_4, \quad (14b)$$

$$Z_3(X) = \bar{X}_1(\bar{X}_2 X_4 \vee X_2 X_3) \vee X_1(X_2 \bar{X}_4 \vee \bar{X}_2 \bar{X}_3) \quad (14c)$$

$$Z_4(X) = X_1 X_3 \vee X_4(X_1 \vee \bar{X}_2), \quad (14d)$$

$$Z_5(X) = \bar{X}_4(X_1 X_3 \vee X_2 \bar{X}_3) \vee \bar{X}_1 X_2 X_3 X_4, \quad (14e)$$

and the required single output for the overall network C is

$$t(X) = \bar{X}_1 \bar{X}_2 \vee \bar{X}_3(\bar{X}_1 \vee \bar{X}_2 \bar{X}_4 \vee X_2 X_4). \quad (15)$$

The information supplied by $Z(X)$ in (14) is equivalent to a single Boolean equation of the form

$$g(X, Z) = \bigwedge_{i=1}^5 (Z_i \odot Z_i(X)) = 1. \quad (16)$$

The function $g(X, Z): B_2^9 \rightarrow B_2$ is viewed as $g(X): B^4 \rightarrow B$, where $B = FB(Z_1, Z_2, Z_3, Z_4, Z_5)$ has 5 generators, $2^5 = 32$ atoms, and $2^{32} = 4,294,967,296$ elements. The natural map for $g(X)$ is shown in Fig. 7. An entry in the cell X of this map is an atom of B of the form $Z_1^{Z_1(X)} Z_2^{Z_2(X)} Z_3^{Z_3(X)} Z_4^{Z_4(X)} Z_5^{Z_5(X)}$. Since $Z_1(X) = X_1$, the literal $Z_1^{Z_1(X)} = Z_1^{X_1}$ is Z_1 when $X_1 = 1$ and $\bar{Z}_1$ when $X_1 = 0$. For convenience, the map demonstrates the construction of $Z_3^{Z_3(X)}$ (as an example) by showing the loops of $Z_3(X)$ in (14c), so that $Z_3(X)$ appears as Z_3 inside these loops and as $\bar{Z}_3$ outside them. Out of the 32 atoms of B , the atom $Z_1 Z_2 \bar{Z}_3 Z_4 \bar{Z}_5$ has two appearances in Fig. 7, which are each appended by one of the orthonormal tags p_1 and $\bar{p}_1$ in Fig. 8, for the auxiliary function, while the atom $\bar{Z}_1 \bar{Z}_2 \bar{Z}_3 \bar{Z}_4 \bar{Z}_5$ has three appearances in Fig. 7, which are each ANDed with one of the orthonormal tags, p_2 , $\bar{p}_2 p_3$ and $\bar{p}_2 \bar{p}_3$ in Fig. 8, where each of p_1 , p_2 and $p_3 \in B_2$ [6, 16]. There are 11 other atoms with a single appearance in Fig. 7, which are each tagged by (1) in Fig. 8, while the remaining 19 atoms do not appear at all in Fig. 7, and must be nullified as a consistency condition and further entered don't-care in the cells of Fig. 8. There are $2^3 = 6$ particular solutions for X . Fig. 9 shows solutions for the X variables, their complements, and their products, culminating in a map for $s = t$ where t is given by (15). Note that the three parameters p_1 , p_2 and p_3 disappeared from the final map for s , which makes s parametrically unique (albeit incompletely specified). The map for s in Fig. 9(l) is particularly covered by the two essential prime-implicant dotted loops $\bar{Z}_1 Z_4$ and $\bar{Z}_2 \bar{Z}_3$ (shown solid). To complete the coverage of s , either of the dotted non-essential loops $Z_1 \bar{Z}_4 \bar{Z}_5$ or $Z_2 \bar{Z}_4 \bar{Z}_5$ is needed. Hence, there are two minimal solutions of s .

$$s = \bar{Z}_1 Z_4 \vee \bar{Z}_2 \bar{Z}_3 \vee Z_1 \bar{Z}_4 \bar{Z}_5, \quad (17a)$$

$$s = \bar{Z}_1 Z_4 \vee \bar{Z}_2 \bar{Z}_3 \vee Z_2 \bar{Z}_4 \bar{Z}_5, \quad (17b)$$

in agreement with the results of Bell [3].

Now, we consider the second method for this example. Figure 10 represents the map for $t(X)$ in (15), while Fig. 11 utilises Fig. 7 (and its complement) together with Fig. 10 to produce a map for $t(X, Z)$, which can be used to find a sneaky translator. However, we note that an honest translator is possible since none of the 32 atoms of $FB(Z_1, Z_2, Z_3, Z_4, Z_5)$ has a mixed assertion in Fig. 11. In fact, there are 6 atoms

that are asserted positively, 7 atoms that are asserted negatively, and 19 atoms asserted neither way. Hence s can be made an honest translator as a disjunction of the 6 positively asserted atoms and, possibly, any of the totally don't-care (non-asserted) atoms. This precisely expresses s by the map in Fig. 9(l), thereby recovering our earlier results.

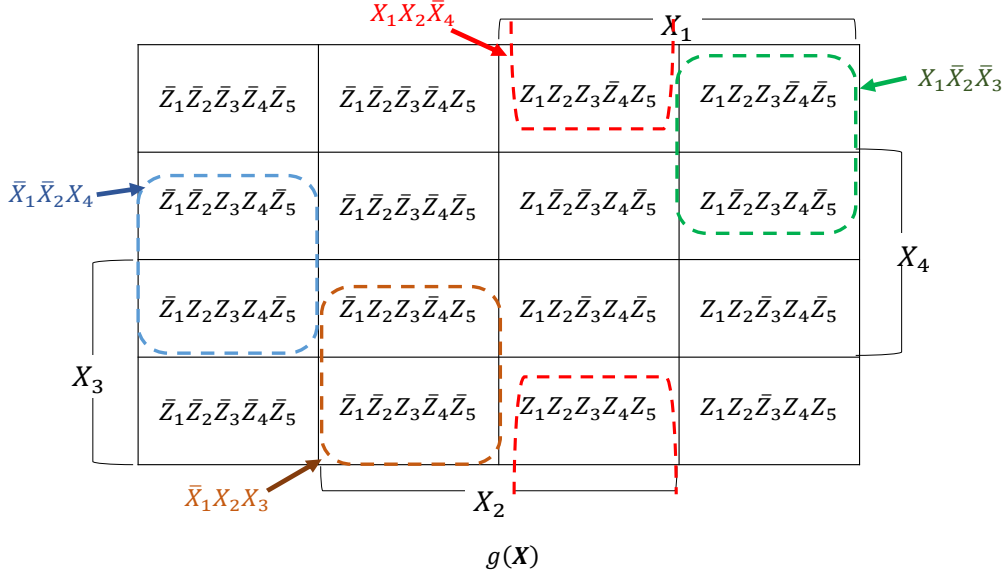


Fig. 7. The natural map for $g(X)$ in (16). Loops for $Z_3(X)$ are shown, inside which Z_3 appears and outside which $\bar{Z}_3$ appears

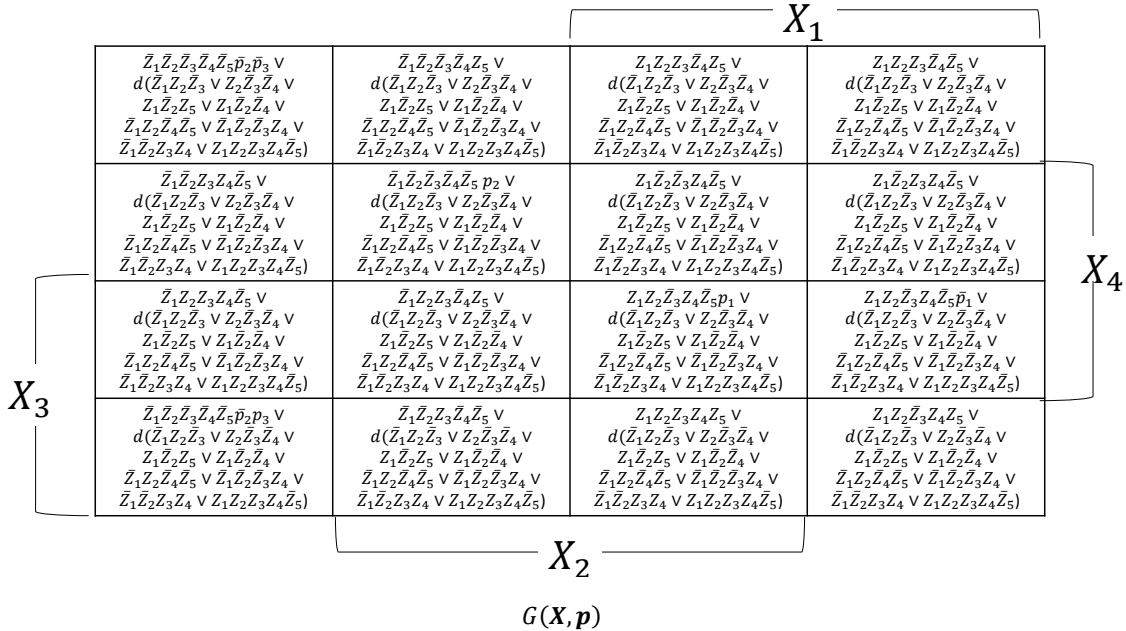


Fig. 8. The auxiliary function used to derive the parametric solutions of $g(X) = 1$ in Section 3.

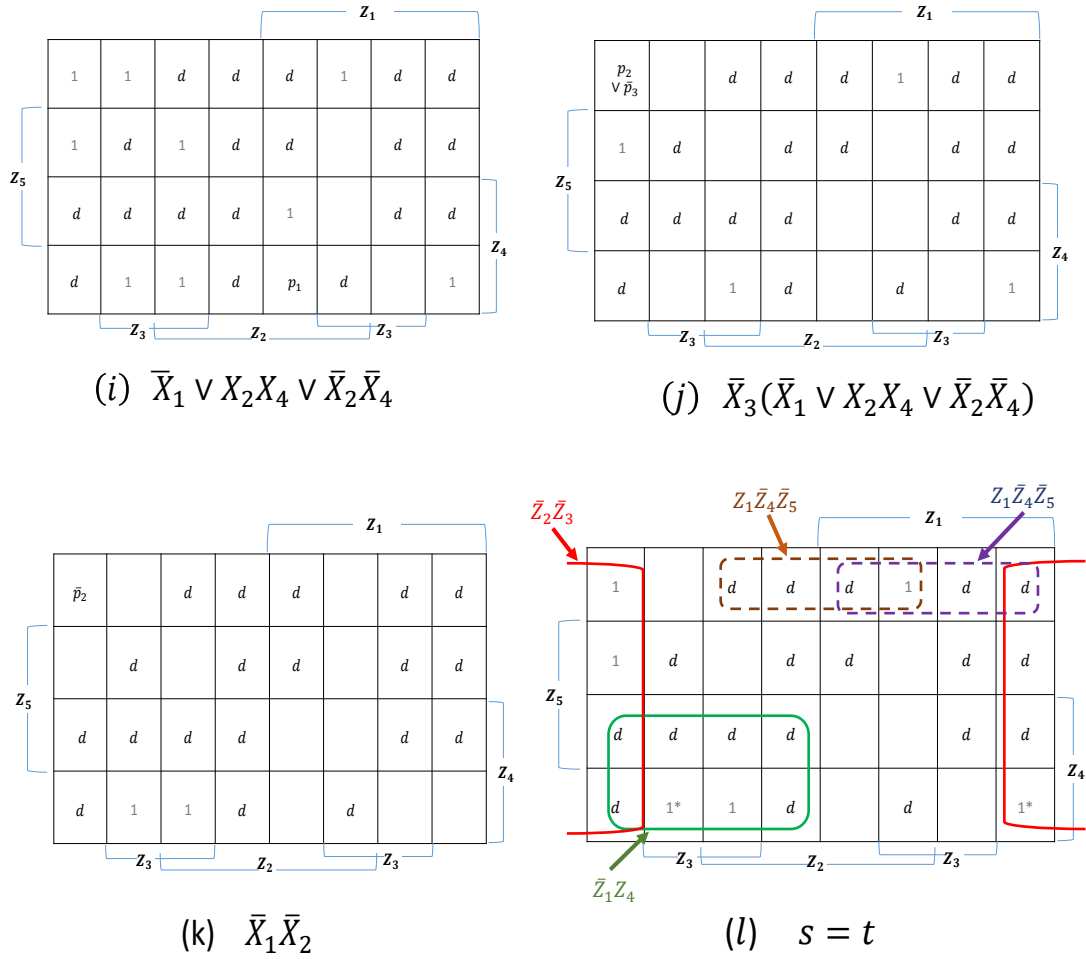


Fig. 9. Solutions for the pertinent X variables, their complements and products in Section 3, culminating in a map for $s = t$ as given by Equation (15)

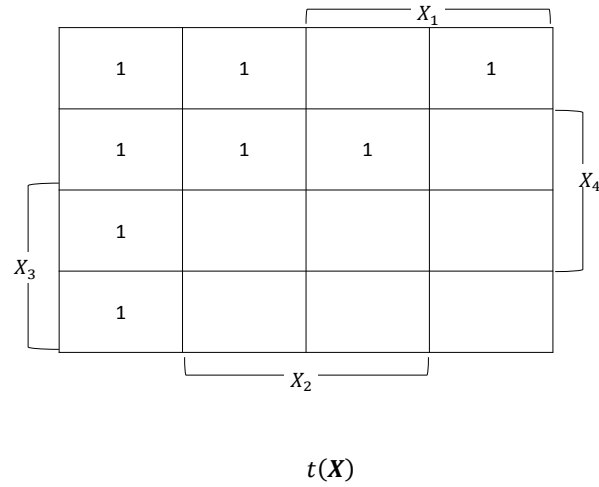


Fig. 10. Conventional Karnaugh map for $t(X)$ expressed by Equation (15) in Section 3

X_3		X_1				X_4
		$\bar{Z}_1\bar{Z}_2\bar{Z}_3\bar{Z}_4\bar{Z}_5$ $\vee d(1)$	$\bar{Z}_1\bar{Z}_2\bar{Z}_3\bar{Z}_4Z_5$ $\vee d(1)$	$d(\bar{Z}_1 \vee \bar{Z}_2 \vee \bar{Z}_3$ $\vee Z_4 \vee \bar{Z}_5)$	$Z_1Z_2Z_3\bar{Z}_4\bar{Z}_5$ $\vee d(1)$	
		$\bar{Z}_1\bar{Z}_2Z_3\bar{Z}_4\bar{Z}_5$ $\vee d(1)$	$\bar{Z}_1\bar{Z}_2\bar{Z}_3\bar{Z}_4\bar{Z}_5$ $\vee d(1)$	$Z_1\bar{Z}_2\bar{Z}_3Z_4\bar{Z}_5$ $\vee d(1)$	$d(\bar{Z}_1 \vee Z_2 \vee \bar{Z}_3$ $\vee \bar{Z}_4 \vee Z_5)$	
		$\bar{Z}_1Z_2Z_3Z_4\bar{Z}_5$ $\vee d(1)$	$d(Z_1 \vee \bar{Z}_2 \vee \bar{Z}_3$ $\vee Z_4 \vee \bar{Z}_5)$	$d(\bar{Z}_1 \vee \bar{Z}_2 \vee Z_3$ $\vee \bar{Z}_4 \vee Z_5)$	$d(\bar{Z}_1 \vee \bar{Z}_2 \vee Z_3$ $\vee \bar{Z}_4 \vee Z_5)$	
		X_2				
		$\bar{Z}_1\bar{Z}_2\bar{Z}_3\bar{Z}_4\bar{Z}_5$ $\vee d(1)$	$d(Z_1 \vee Z_2 \vee \bar{Z}_3$ $\vee Z_4 \vee Z_5)$	$d(\bar{Z}_1 \vee \bar{Z}_2 \vee Z_3$ $\vee \bar{Z}_4 \vee \bar{Z}_5)$	$d(\bar{Z}_1 \vee \bar{Z}_2 \vee Z_3$ $\vee \bar{Z}_4 \vee \bar{Z}_5)$	

$$s(\mathbf{X}, \mathbf{Z}) = tg \vee d(\bar{g})$$

Fig. 11. Natural map for $s(\mathbf{X}, \mathbf{Z})$ in Section 3

4. A CIRCUIT EXAMPLE WITH SIDE INPUT

This example was solved earlier by Ledley [2] and Brown [4] and differs from the earlier two examples, since it has side inputs $\mathbf{Y}$. The example is specified by:

$$t(\mathbf{X}, \mathbf{Y}) = X_1X_2 \vee Y_1\bar{X}_2X_3 \vee Y_2(X_1\bar{X}_3 \vee X_2), \quad (18)$$

$$\mathbf{Z}(\mathbf{X}) = \begin{bmatrix} X_1\bar{X}_2 \vee \bar{X}_1X_3 \\ \bar{X}_1X_2 \vee X_1\bar{X}_3 \\ X_1X_2 \vee \bar{X}_2X_3 \end{bmatrix}. \quad (19)$$

We rewrite (19) in equational form as

$$g(\mathbf{X}, \mathbf{Z}) = (Z_1 \odot (X_1\bar{X}_2 \vee \bar{X}_1X_3))(Z_2 \odot X_1X_2 \vee X_1X_3Z_3 \odot X_1X_2 \vee X_2X_3 = 1) \quad (20)$$

and proceed to solve it for $\mathbf{X}$ in terms of $\mathbf{Z}$. In Figs (12a)-(12c), we draw maps of the factors in (19), and then AND them cell-wise to draw the natural map of g as a function of $\mathbf{X}$ over the big Boolean algebra $FB(Z_1, Z_2, Z_3)$. Fig. 12(d) shows that four atoms of $FB(Z_1, Z_2, Z_3)$, namely $\bar{Z}_1\bar{Z}_2\bar{Z}_3$, $\bar{Z}_1Z_2\bar{Z}_3$, $\bar{Z}_1Z_2Z_3$, and $\bar{Z}_1\bar{Z}_2Z_3$ appear once each, and two atoms, viz., $Z_1\bar{Z}_2\bar{Z}_3$, and $Z_1Z_2\bar{Z}_3$ appear twice each, while the remaining two atoms ($Z_1Z_2Z_3$, and $Z_1\bar{Z}_2Z_3$) never appear. This means that the consistency condition is

$$Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3 = 0, \quad (21)$$

and the number of particular solutions subject to that condition is $(1)^4(2)^2 = 4$. The auxiliary function $G(\mathbf{X}, \mathbf{p})$ is shown in Fig. 13 where we used a parameter p_1 to create orthonormal tags $\{p_1, \bar{p}_1\}$ for the atom $Z_1Z_2\bar{Z}_3$, and an independent parameter p_2 to create orthonormal tags $\{p_2, \bar{p}_2\}$ for the atom $Z_1\bar{Z}_2Z_3$. From Fig. 13, we obtain the following expressions for the $\mathbf{X}$ variables and some of their complements

$$X_1 = \bar{Z}_1Z_3 \vee Z_1Z_2\bar{Z}_3\bar{p}_1 \vee Z_1\bar{Z}_2Z_3p_2 \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3), \quad (22a)$$

$$X_2 = \bar{Z}_1Z_3 \vee \bar{Z}_1Z_2 \vee Z_1Z_2\bar{Z}_3p_1 \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3), \quad (22b)$$

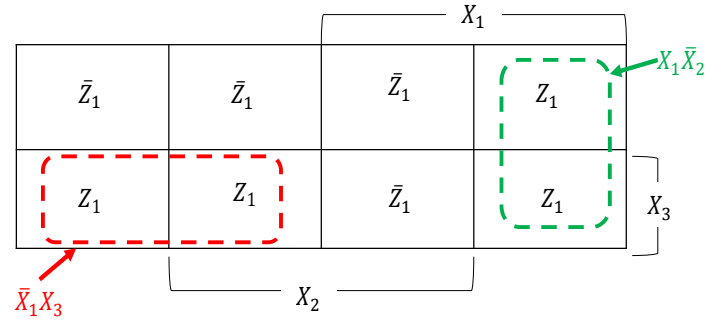
$$X_3 = \bar{Z}_2Z_3 \vee Z_1Z_2\bar{Z}_3p_1 \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3), \quad (22c)$$

$$\bar{X}_2 = \bar{Z}_1\bar{Z}_2\bar{Z}_3 \vee Z_1Z_2\bar{Z}_3\bar{p}_1 \vee Z_1\bar{Z}_2Z_3 \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3), \quad (22d)$$

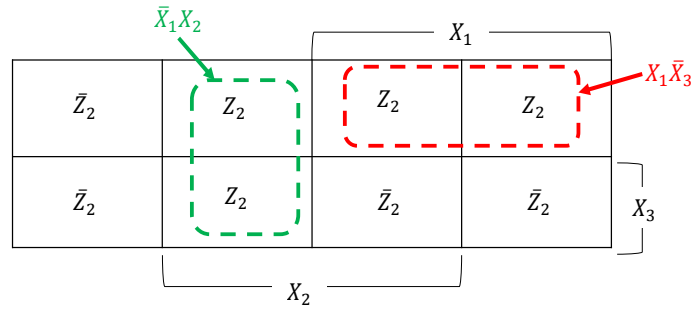
$$\bar{X}_3 = \bar{Z}_1\bar{Z}_3 \vee \bar{Z}_1Z_2 \vee Z_1Z_2\bar{Z}_3\bar{p}_1 \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3). \quad (22e)$$

Finally, $t(\mathbf{X}, \mathbf{Y})$ in (18) is replaced by $s(\mathbf{Z}, \mathbf{Y})$, using intelligent multiplication [28-34]

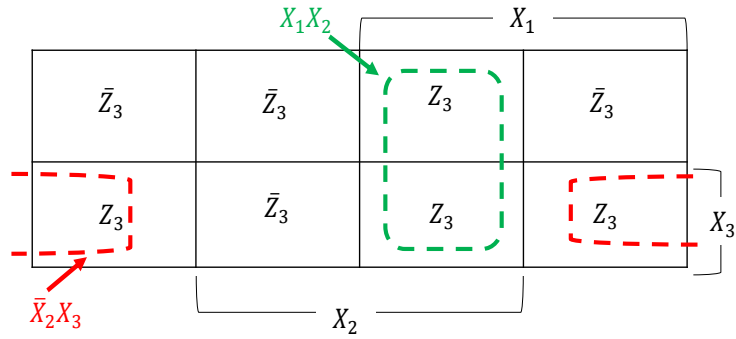
$$s(\mathbf{Z}, \mathbf{Y}) = \bar{Z}_1Z_3 \vee Y_1Z_1\bar{Z}_2Z_3 \vee Y_2(\bar{Z}_1Z_2 \vee Z_2\bar{Z}_3) \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3) \quad (23)$$



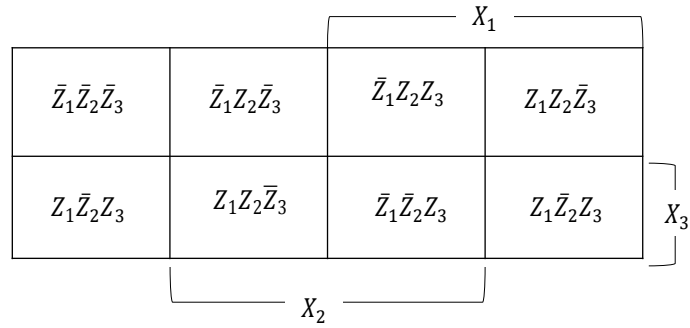
$$\mathbf{A) } Z_1 \odot Z_1(X) = Z_1 \odot (X_1\bar{X}_2 \vee \bar{X}_1X_3)$$



$$\mathbf{B) } Z_2 \odot Z_2(X) = Z_2 \odot (\bar{X}_1X_2 \vee X_1\bar{X}_3)$$



$$\mathbf{C) } Z_3 \odot Z_3(X) = Z_3 \odot (X_1X_2 \vee \bar{X}_2X_3)$$



$$\mathbf{D) } g(X)$$

Fig. 12. Gradual derivation of the natural map of $g(X)$ of in Section 4

		X_1		
$\bar{Z}_1\bar{Z}_2\bar{Z}_3(1) \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3)$	$\bar{Z}_1Z_2\bar{Z}_3(1) \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3)$	$\bar{Z}_1Z_2Z_3(1) \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3)$	$Z_1Z_2\bar{Z}_3(\bar{p}_1) \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3)$	
$Z_1\bar{Z}_2Z_3(\bar{p}_2) \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3)$	$Z_1Z_2\bar{Z}_3(p_1) \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3)$	$\bar{Z}_1\bar{Z}_2Z_3(1) \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3)$	$Z_1\bar{Z}_2Z_3(p_2) \vee d(Z_1Z_2Z_3 \vee Z_1\bar{Z}_2\bar{Z}_3)$	X_3
X_2				

$G(X, p)$

Fig. 13. The auxiliary function needed in Section 4

The function $s(Z, Y)$ is represented by the VEKM of Fig. 14, which can be read to yield the minimal expression (obtained earlier by Brown [4])

$$s(Z, Y) = \bar{Z}_1Z_3 \vee Y_1Z_3 \vee Y_2Z_2. \quad (24)$$

Fig. 14 can also be used to verify the non-minimal solution obtained by Ledley [2]

$$s(Z, Y) = \bar{Z}_1Z_3 \vee Y_1Z_1\bar{Z}_2 \vee Y_2Z_2\bar{Z}_3. \quad (25)$$

Now, we consider the second method for this example. Fig. 15 represents a VEKM for $t(X, Y)$ in (18). When one utilises Fig. 12(d) (and its complement) to produce a representation of $s = tg \vee d(\bar{g})$, Fig. 16 is simply obtained.

		Z_1		
0	Y_2	Y_2	d	
$\bar{Z}_1Z_3$	1	1	d	Z_3
Z_3		Z_2		

$s(Z, Y)$

Fig. 14. A VEKM representation for $s(Z, Y)$ in Section 4

		X_1		
0	Y_2	1	Y_2	
Y_1	Y_2	1	Y_1	X_3
X_2				

$t(X, Y)$

Fig. 15. A VEKM representing $t(X, Y)$ in (18) of Section 4

X_1			
$d(Z_1 \vee Z_2 \vee Z_3)$	$Y_2 \bar{Z}_1 Z_2 \bar{Z}_3 \vee$ $d(Z_1 \vee \bar{Z}_2 \vee Z_3)$	$\bar{Z}_1 Z_2 Z_3 \vee$ $d(1)$	$Y_2 Z_1 Z_2 \bar{Z}_3 \vee$ $d(\bar{Z}_1 \vee \bar{Z}_2 \vee Z_3)$
$Y_1 Z_1 \bar{Z}_2 Z_3 \vee$ $d(\bar{Z}_1 \vee Z_2 \vee \bar{Z}_3)$	$Y_2 Z_1 Z_2 \bar{Z}_3 \vee$ $d(\bar{Z}_1 \vee \bar{Z}_2 \vee Z_3)$	$\bar{Z}_1 \bar{Z}_2 Z_3 \vee$ $d(1)$	$Y_1 Z_1 \bar{Z}_2 Z_3 \vee$ $d(Z_1 \vee \bar{Z}_2 \vee Z_3)$
X_2			

X_3

$$s(X, Y, Z) = tg \vee d(\bar{g})$$

Fig. 16. A VEKM representing $s(X, Y, Z)$ in Section 4

With $s(X, Y, Z)$ viewed as $s(X): B^3 \rightarrow B$, where $B = FB(Z_1, Z_2, Z_3, Y_1, Y_2)$ has 32 atoms. Again, none of these atoms (which can be viewed as the cell products of the 5-variable Karnaugh map in Fig. 17 has a mixed assertion. In fact, we are forced to enter a single entry of 1 in 14 cells of the map in Fig. 17, to enter a unique 0 entry in 10

cells of that map, and to leave 8 cells intact (presumably don't-cares). This means that $s(X, Y, Z)$ can be represented by the map in Fig. 17 as $s(Z, Y)$ independently of X , and it has the minimal coverage depicted by the three loops in Fig. 17 which corresponds to the expression (24).

Z_1							
0	1*	1	0	0	d	0	d
0	1	1	1	1	d	0	d
0	1	1	1*	1	d	1	d
0	1	1	0	0	d	1	d
Z_3 Z_2 Z_3							

$s(Z, Y)$

Fig. 17. A 5-variable Karnaugh map for admitting a representation of $s(X, Y, Z)$ that is independent of X

Table 1. Comparison of the methods of Boolean-equation solving and input-domain constraining

	Boolean-equation solving	Input-domain constraining
Scope	A general-purpose technique	A special-purpose technique
Utility	Useful for a wide variety of applications including the Type-2 and Type-3 problems	Particularly tailored to the Type-2 problem
Efficiency	Relatively less efficient as it produces parameters that ultimately disappear	Relatively more efficient as it does not include any unwarranted steps
Potential as a replacement to the conventional method	A good replacement due to its simplicity, insightfulness, and generality	A good replacement due to its simplicity, insightfulness, and speed

5. DISCUSSION

This paper is a part of our own consolidated effort to modernise certain techniques for handling fundamental problems of digital circuit design. These efforts are just a modest supplement to extensive efforts by the digital-design community [35-48]. We devote this paper to handling what is called Type-2 problems, with our sister publication [6] dedicated to Type-3 problems. While our treatment of Type-3 problems in [6] relied solely on equation-solving in big Boolean algebras, we considered herein a similar treatment for Type-2 problems, but we exposed it in comparison with another method [5] that adapts the input-domain constraining technique *via* utilisation of variable-entered Karnaugh map (VEKMs) together with modern don't-care notation. Our method used in [6] as well as our two methods employed herein outperform the conventional method both in speed and clarity. Our main concern herein is to decide which of our two novel competing methods is preferable. The answer seems to be a matter of personal taste, convenience, and relative experience. There is definitely some similarity, interaction, and conceptual relationship between the two methods. We note that the Boolean-equation-solving method produces parametric solutions that lead to several parametric solutions expressed in terms of a few parameters. However, these parameters disappeared later in the final stage of problem solving. Therefore, the Boolean-equation-solving method seems to involve certain unwarranted steps that might be possibly skipped. However, its utility is not restricted to type-2 problems, since it handles type-3 problems (and many other problems) as well. In all the examples worked out herein, the two methods obtained exactly the same answers. These answers agreed with (or occasionally were more compact

than) answers obtained conventionally. Table 1 summarises our comparison of the two methods of Boolean-equation solving and input-domain constraining.

6. CONCLUSIONS

This paper exposed, illustrated, and compared the two methods of Boolean-equation solving and input-domain constraining, which are novel methods for handling Type-2 problems of digital circuit design. The paper demonstrated the superiority of these two methods to (as well as agreement with) the old conventional method. Three typical classical examples are presented, for which known conventional solutions are somewhat tedious and cumbersome, while the modern solutions presented herein are simple and insightful. Throughout these examples, the Karnaugh map is effectively utilised, either in its conventional version or in its variable-entered version.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Ledley, R. S., Boolean matrix equations in digital circuit design, *IRE Transactions on Electronic Computers*, Vol. EC-8, No. 6, (1959), pp. 131-139.
2. Ledley, R. S. *Digital Computer and Control Engineering*. McGraw-Hill, New York, NY, USA (1960).
3. Bell, N. R., A map method for the teaching of the fundamental concepts of compound-input logic circuits. *IEEE Transactions on Education*, Vol. 11, No. 3, (1968), pp. 173-177.

4. Brown, F. M., The constrained-input problem, *IEEE Transactions on Computers*, Vol. C-24, No. 1, (1975), pp. 102-106.
5. Rushdi A. M. A., Handling generalized type-2 problems of digital circuit design via the variable-entered Karnaugh map, *International Journal of Mathematical, Engineering and Management Sciences (IJMEMS)*, 3(4), (2018).
6. Rushdi, A. M. A and Ahmad, W., Digital circuit design utilizing equation solving over 'big' Boolean equations, *International Journal of Mathematical, Engineering and Management Sciences (IJMEMS)*, 3(4), (2018).
7. Brown, F. M., On the suppression of variables in Boolean equations, *Discrete Applied Mathematics*, Vol. 159, (2011), No. 5, pp. 255-258.
8. Rushdi, A. M. A and Ahmad, W., Satisfiability in 'big' Boolean algebras via Boolean-equation solving, *Journal of King Abdulaziz University: Engineering Sciences*, Vol. 28, No. 1, (2016), pp.3-18.
9. Rushdi, A. M. A and Ahmad, W., A Novel method for compact listing of all particular solutions of a system of Boolean equations, *British Journal of Mathematics & Computer Science*, Vol. 22, No. 6, 1-18. (2017), pp. 1-18.
10. Reusch, B., Generation of prime implicants from subfunctions and a unifying approach to the covering problem. *IEEE Transactions on Computers*, Vol. 100, No. 9, (1975), pp. 924-930.
11. Rushdi, A. M., Improved variable-entered Karnaugh map procedures, *Computer and Electrical Engineering*, Vol. 13, No. 1, (1987), pp. 41-52.
12. Rushdi, A. M., Using variable-entered Karnaugh maps to solve Boolean equations, *International Journal of Computer Mathematics*, Vol. 78, No. 1, (2001), pp. 23-38.
13. Rushdi, A. M., Efficient solution of Boolean equations using variable-entered Karnaugh maps, *Journal of King Abdulaziz University: Engineering Sciences*, Vol. 15, No. 1, (2004), pp. 105-121.
14. Rushdi, A. M. A. and H. M. Albarakati, Prominent classes of the most general subsumptive solutions of Boolean equations, *Information Sciences*, Vol. 281, (2014), pp. 53-65.
15. Rushdi, A. M. and M. H. Amashah, Parametric general solutions of Boolean equations via variable-entered Karnaugh maps, *Journal of Qassim University: Engineering and Computer Sciences*, Vol. 3, No. 1, (2010), pp. 59-71.
16. Rushdi, A. M. and M. H. Amashah, Using variable-entered Karnaugh maps to produce compact parametric general solutions of Boolean equations, *International Journal of Computer Mathematics*, Vol. 88, No. 15, (2011), pp. 3136-3149.
17. Rushdi, A. M., A comparison of algebraic and map methods for solving general Boolean equations, *Journal of Qassim University: Engineering and Computer Sciences*, Vol. 5, No. 2, (2012), pp. 147-173.
18. Rushdi, A. M. and M. H. Amashah, Purely-algebraic versus VEKM methods for solving big Boolean equations, *Journal of King Abdulaziz University: Engineering Sciences*, Vol. 23, No. 2, (2012), pp. 75-85.
19. Rushdi, A. M. A., and Albarakati, H. M., Construction of general subsumptive solutions of Boolean equations via complete-sum derivation, *Journal of Mathematics and Statistics*, Vol. 10, No. 2, (2014), pp. 155-168.
20. Rushdi A. M. A., and Al-Qwasmi, M., Formal derivation of a particular input of a single AND (OR) gate in terms of its output and other inputs, *Journal of King Abdulaziz University: Engineering Sciences*, Vol. 26, No. 2 (2016), pp. 51-62.
21. Rushdi, A. M., and Zagzoog, S. S., Design of a digital circuit for integer factorization via solving the inverse problem of logic, *Journal of Advances in Mathematics and Computer Science*, Vol. 26, No. 3, (2018), pp. 1-14.
22. Rushdi, A. M., and Zagzoog, S. S., Derivation of all particular solutions of a 'big' Boolean equation with applications in digital design, *Current Journal of Applied Science and Technology*, Vol. 27, No. 3, (2018), pp. 1-16.
23. Rushdi, A. M., Zagzoog, S. S., and Balamesh, A. S. Design of a hardware circuit for integer factorization using a big Boolean algebra, *Journal of Advances in Mathematics and Computer Science*, Vol. 27, No. 1, (2018), pp. 1-25.
24. Ahmad W, Rushdi, A. M. A., A new cryptographic scheme utilizing the difficulty of big Boolean satisfiability, *International Journal of Mathematical, Engineering and*

- Management Sciences (IJMEMS)*, Vol. 3, No. 1, (2018), pp. 47-61.
25. Rushdi, A. M., & Balamesh, A. S. On the relation between Boolean Curve Fitting and the Inverse Problem of Boolean Equations. *Journal of King Abdulaziz University: Engineering Sciences*, Vol. 28, No. 2 (2018), pp. 3-9.
26. Rushdi, A. M. and Al-Yahya, H. A., A Boolean minimization procedure using the variable-entered Karnaugh map and the generalized consensus concept, *International Journal of Electronics*, Vol. 87, No. 7, (2000), pp. 769-794.
27. Rushdi, A. M. and Al-Yahya, H. A., Further improved variable-entered Karnaugh map procedures for obtaining the irredundant forms of an incompletely-specified switching function, *Journal of King Abdulaziz University: Engineering Sciences*, Vol. 13, No. 1, (2001), pp. 111-152.
28. Brown, F. M., *Boolean Reasoning, the Logic of Boolean Equations*, Kluwer Academic Publisher, Boston, MA, USA (1990).
29. Rushdi, A. M., and Al-Yahya, H. A., Derivation of the complete sum of a switching function with the aid of the variable-entered Karnaugh map, *Journal of King Saud University: Engineering Sciences*, Vol. 13, No. 2, (2001), pp. 239-269.
30. Rushdi, A. M. and Rushdi, M. A., Switching-Algebraic Analysis of System Reliability, Chapter 6 in Ram, M. and Davim, P. (Editors), *Advances in Reliability and system Engineering*, Springer, Cham, Switzerland (2017), pp. 139-161.
31. Rushdi A. M. A., and Ahmad, W., Finding all solutions of the Boolean satisfiability problem, if any, via Boolean-equation solving, *Journal of King Abdulaziz University: Engineering Sciences*, Vol. 27, No. 1 (2017), pp. 19-34.
32. Ahmad W, Rushdi, A. M. A., A novel minimization method for sensor deployment via heuristic 2-sat solution, *Sir Syed University Research Journal of Engineering & Technology*, Vol.7, No. 1, (2017), pp. 1-7.
33. Rushdi, R, A., and Rushdi, A. M, Karnaugh-map utility in medical studies: The case of Fetal Malnutrition, *International Journal of Mathematical, Engineering and Management Sciences (IJMEMS)*, Vol. 3, No. 3, (2018), pp. 220-244.
34. Rushdi, M. A., Rushdi, A. M., Zarouan, M., and Ahmad, W. (2018). Satisfiability in intuitionistic fuzzy logic with realistic tautology, *Kuwait Journal of Science (KJS)*, Vol. 45, No. 2 (2018), 15-21.
35. Wang, H. (1959). Circuit synthesis by solving sequential Boolean equations. *Mathematical Logic Quarterly*, 5(14-24), 291-322.
36. Brown, F. M. (1974). Equational logic. *IEEE Transactions on Computers*, C-23(12), 1228-1237.
37. Brown, F. M. (1975). Weighted Realizations of Switching Functions. *IEEE Transactions on Computers*, C-24(12), 1217-1221.
38. Brown, F. M. (1975). Equational realizations of switching functions. *IEEE Transactions on Computers*, C-24(11), 1054-1066.
39. Wang, Y., & McCrosky, C. (1998). Solving Boolean equations using ROSOP forms. *IEEE Transactions on Computers*, 47(2), 171-177.
40. Rushdi, A. M., & Ba-Rukab, O. M. (2003). Low-cost design of multiple-output switching circuits using map solutions of Boolean equations. *Umm AL-Qura University Journal: Science Medicine & Engineering* 15(2), 59-79.
41. Navabi, Z. (2004). *Digital design and Implementation with Field Programmable Devices*. Springer Science & Business Media.
42. Nedjah, N., & de Macedo Mourelle, L. (2004, May). A comparison of two circuit representations for evolutionary digital circuit design. In *International Conference on Industrial, Engineering and Other Applications of Applied Intelligent Systems* (pp. 594-604). Springer, Berlin, Heidelberg.
43. Katz, R. H., & Borriello, G. (2005). *Contemporary Logic Design*, Second Edition, Pearson Education, Upper Saddle River, New Jersey, USA.
44. Horowitz, M., Stark, D., & Alon, E. (2008). Digital circuit design trends. *IEEE Journal of Solid-State Circuits*, 43(4), 757-761.
45. Horowitz, M., Stark, D., & Alon, E. (2008). Digital circuit design trends. *IEEE Journal of Solid-State Circuits*, 43(4), 757-761.
46. Fakhfakh, M., Tlelo-Cuautle, E., & Siarry, P. (Eds.). (2015). *Computational Intelligence in Digital and Network Designs*

- and Applications*. Springer International Publishing.
47. Llorente, C. (2017). Outcome-based Approach in Teaching Digital Systems Design for Undergraduate Computer and Electronics Engineering Programs. *Journal of Telecommunication, Electronic and Computer Engineering (JTEC)*, 9(2-8), 113-118.
 48. Donzellini, G., Oneto, L., Ponta, D., & Anguita, D. (2019). Combinational Network Design. In *Introduction to Digital Systems Design* (pp. 33-78). Springer, Cham.